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DEVELOPMENT OF TRANSISTORIZED SOLID STATE POWER CONTROLLERS FOR--ETC(U)
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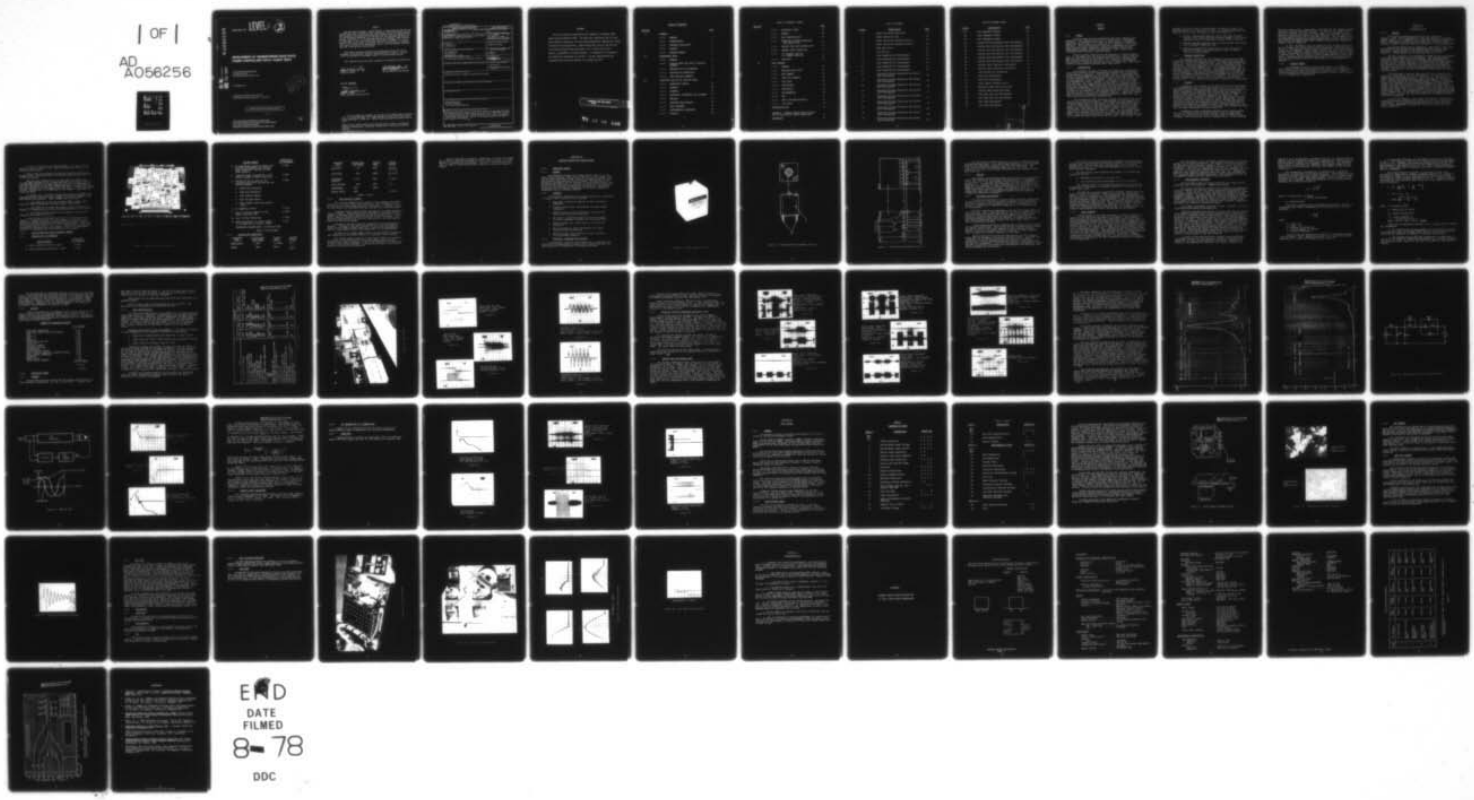

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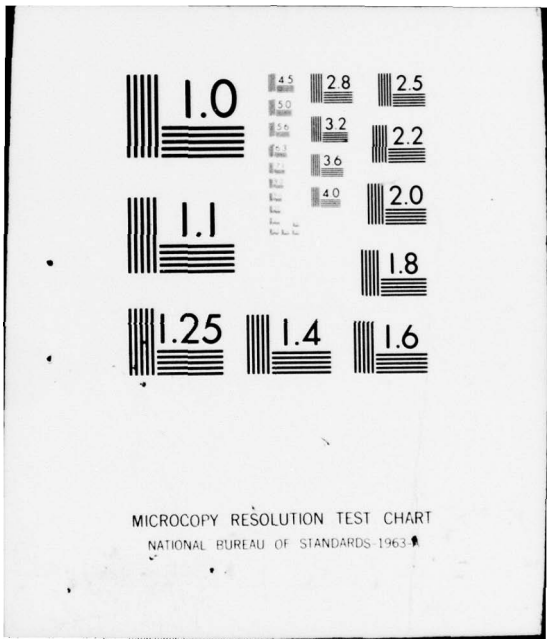
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LEVEL II

B.S. 2

DEVELOPMENT OF TRANSISTORIZED SOLID STATE POWER CONTROLLERS FOR B-1 FLIGHT TESTS

TELEPHONICS CORPORATION
770 PARK AVENUE
HUNTINGTON, NEW YORK 11743

NOVEMBER 1977

TECHNICAL REPORT AFAPL-TR-77-67
Final Report for Period January 1974 – June 1977

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Fifty-nine transistorized solid state power controllers have been developed, fabricated and tested. These devices are rated at 1.6 A/230V/400Hz, possess the control/protect functions, are hermetically sealed, and are packaged in a flight worthy configuration. Details of the design, assembly, and testing are included in this report.

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FOREWORD

This final report was submitted by ISC Telephonics in February 1978 under contract F33615-74-C-2031. The effort was sponsored by the Air Force Aero Propulsion Laboratory, Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, under Project 3145, Task 29, and Work Unit 49 ("Transistorized AC Power Controllers for B-1 Flight Test") with Edmond J. Caputo/POP-2 as Project Engineer. G. Altemose of ISC Telephonics was technically responsible for the work. The work reported herein was performed during the period January 1974 through June 1977.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT)

LIST OF FIGURES

LIST OF FIGURES (CONT)

SECTION I

SUMMARY

1.1.0 GENERAL

Transistorized AC Power Controllers have been developed and produced in this program for use in B-1 flight tests. Each power controller is suitable for any class of load (resistive, inductive, capacitive, motor, lamp, etc.) rated up to 1.6 amperes, at 230 volts, 400 hertz. The Power Controllers have been comprehensively tested under extreme stress conditions, including voltage fluctuations, temperature extremes, nuclear susceptibility, EMI, various loads (including short circuits), and life tests.

Fifty nine Power Controllers were produced in sealed aluminum cans, in accordance with the original specification. Late in the program two Power Controller printed circuit cards were developed with four Power Controllers on each card, to be compatible with Rockwell International's packaging concept for the B-1, which used a Load Center instead of distributed individual Power Controllers.

1.2.0 INTRODUCTION

The dramatic increases in weight and complexity of electrical distribution systems in new aircraft have dictated that a new power system design be developed. Such designs utilize a multiplexed data system with programmable logic and solid state power controllers. All of this hardware, with the exception of solid state power controllers, is being applied to the B-1 aircraft. Presently, the B-1 is using electromechanical relays, thermal circuit breakers, and solid state relay drivers. The relay drivers are required to interface between the electrical multiplex (EMUX) system and the electromechanical relays. While many advantages of the new system are realized by the utilization of EMUX, its full potential will not be reached until solid state power controllers are available. The problems present with solid state power controllers were their circuit complexity and cost. Additional development was needed to simplify the circuit complexity, reduce cost, and ensure power controller/load compatibility.

The Telephonics power controller designs are based on the use of transistors as the pass elements. Many designs of high powered AC controllers employ SCR's for the control of high current/voltage loads. In the B-1 application a high voltage of 230 volts, 400 Hz is used to reduce the load currents, and thus provide weight reduction in the wiring area. Thus many loads draw small currents. It is estimated that over 50% of the loads are under 0.5 amps. In this current range, commercially available transistors can provide many advantages over SCR's. They provide protection for wiring in the loads as well as the wire between the power controllers and the loads. This feature is most

desirable on the B-1 where, because weight is highly critical, the smallest possible size wire will be used. The primary advantages and characteristics of the Telephonics transistor design are:

- Current limiting and rapid cut off in less than 30 micro-seconds, above 1000% overload, prevents damage to wiring and components within the many small current loads in the B-1.
- Provides failsafe operation for full and partial load shorts with a standard commercial fuse.
- Efficient operation with smaller wire sizes which may be used in the future for small loads in order to reduce critical aircraft weight.

1.3.0 CONTRACT OBJECTIVES

The original objective of this program as stated in the SOW is to provide flightworthy prototype 230 volt AC power controllers for flight test on the third RDT&E aircraft. The program was divided into two phases. They were described in the SOW as a breadboard phase to "consist of building breadboard solid state power controllers and checking them for load compatibility. The breadboard design will be modified as required until a design is established that will meet the B-1 requirements." The second or prototype phase is to "consist of taking the design developed in Phase I and packaging it in a flight-worthy configuration for the flight test program." The SOW also required Telephonics to "maintain close coordination with Rockwell International." The complete specification is provided in the Appendix.

1.4.0 HISTORY

Telephonics' first effort in the SPPC field was the development of a breadboard version of a DC Power Controller in 1970. This unit employed a current limiting approach using a transistor and series resistor combination in parallel across the normal pass transistor. Above a preset current overload, the current could be switched to the parallel path where it would be limited by the resistor. The Telephonics effort subsequently shifted to the high voltage AC Power Controller because of the Air Force B-1 bomber application. At that time the SCR was the only pass element used in AC Power Controllers. Telephonics selected the transistor rather than the SCR for this AC application because of its inherent current limiting capability, its ability to be shut off anywhere in the AC cycle (for extreme overloads) and its higher resistance to nuclear radiation.

Telephonics built a breadboard version of the transistorized 230 volt AC power Controller which handled 1 ampere steady-state current and passed turn-on inrush currents of up to 1000% without tripping. Turn on and turn off were accomplished at the zero voltage

and zero current point, respectively, even when the unit tripped because the preset tripout curve was exceeded. If, however, the 1000% overload value was exceeded, the pass transistor came out of saturation, automatically limiting the current to about 1000%, and then the transistor would be rapidly turned off in less than 25 usecs. This breadboard and its characteristics were successfully demonstrated several years ago to the Air Force at WPAFB, NADC, NASA, Rockwell International, Boeing and Douglas Aircraft Companies.

In 1974, Telephonics won the competition for AC Power Controller for B-1 flight test, which called for the development and production of 59 units. The approach, which utilizes transistors as the pass elements limits inrush currents to about 1000% overload, and will trip out within 25 usecs if currents in excess of this value are demanded, such as into a shorted load. The full output voltage is maintained up to this 1000% point. Overloads below this value will cause trip out if they are present for the periods in excess of that shown in the specification in Appendix A.

1.5.0 PROGRAM PHASES

This program consisted of two related phases: (1) PHASE I, which consisted of building breadboard solid state power controllers of the type that would meet established B-1 requirements; (2) PHASE II, which consisted of taking the design developed in PHASE I and packaging it in a flightworthy configuration.

SECTION II

BREADBOARD PHASE

2.1.0 SUMMARY

The original breadboard phase of the job started on January 2, 1974. The requirements at that time included a full-load current capacity of 1.5 amperes with a time-trip curve up to 1400% overload at which point instant trip-out would occur. This was later lowered to 1000% to coincide with more realistic B-1 load requirements.

The package design was an inseparable, completely potted assembly mounted by two captive screws through opposite corners. All electrical connections were to be made by way of a top-mounted connector. Target weight for the prototype unit was 3 oz.

The basic premise of the Telephonics design was the use of monolithic Darlington chips as the pass element. The overload current requirement could only be met by connecting three Darlingtons in parallel in each current direction. The transistors are used basically as high current switches operating at either cut-off or saturation. This affords high current capacity, low voltage drop (and power dissipation) and sub-cycle control enabling interruption of excessive current at any point in the cycle, providing a high degree of load and wire protection.

The design which resulted from this was a unit which met the electrical requirements, but was over-weight (9 oz.) and projected an impractically high production cost. Since this was unacceptable to AFAPL, several new design directions were investigated. The result was a reinitialization of the breadboard phase to develop a prototype design that eliminated the use of potting compound (a major source of weight) and replaced the proposed custom hybrids with a monolithic circuit approach, resulting in a cost and weight reduction. Full load current was raised from 1.5 to 1.6 amperes with the instant trip level remaining at 1000%. The configuration of the package remained the same with a hermetic seal at the base/cover/connector interfaces required to compensate for the fact that the unit would not be completely filled with potting compound.

Late in the program it was evident that Rockwell International's packaging concept had evolved into printed circuit card versions for load control. This resulted from the decision to utilize the "load center" power management system rather than distributed individual power controllers.

To meet the objective of producing SSPC's for use on the B-1 aircraft, printed circuit cards, each containing four SSPC's, were fabricated and tested.

These cards were designed and fabricated during October and November 1976. The cards used an electrical circuit nearly identical to the can version.

The time-trip characteristic of each SSPC was modified for 2.0 amps RMS, instead of the 1.6 amps RMS used in the cans. The card performed successfully and demonstrated that a very low temperature rise was achieved by using thin aluminum overlays to conduct heat from the pass transistors to the edge of the card where, in the final configuration, the heat will be transferred to the chassis. This card was tested at WPAFB.

In January 1977, technical discussions with RI and WPAFB engineering personnel disclosed that a number of technical changes in the SSPC design were required. These changes were as follows:

a. Each SSPC was to have an isolated STATUS output, which should be derived from output voltage, rather than current.

b. Each SSPC was to have a DC output, capable of 200 milliamperes, by connecting a full wave diode bridge across the AC output.

c. Each SSPC should be able to be configured from the I/O connector as either N.O. or N.C.

A new design was developed, and a new card fabricated (see figure 1), incorporating all of these changes. In addition, the design was further modified to include PIN diode optical couplers, which has previously passed the B-1 nuclear requirements. The size of this new card is 6.75" x 7.6" x 0.6." The complete card has been successfully demonstrated to RI personnel, both at the Telephonics facility in Huntington and the RI offices in Los Angeles.

2.2.0 FAILURE MODE AND EFFECT ANALYSIS SUMMARY

2.2.1 PROBABILITY OF OCCURRENCE

FAILURE EFFECT	PROBABILITY OF OCCURRENCE
1) Loss of power controller output.	0.0505
2) Half waving when controller is OFF.	0.2074

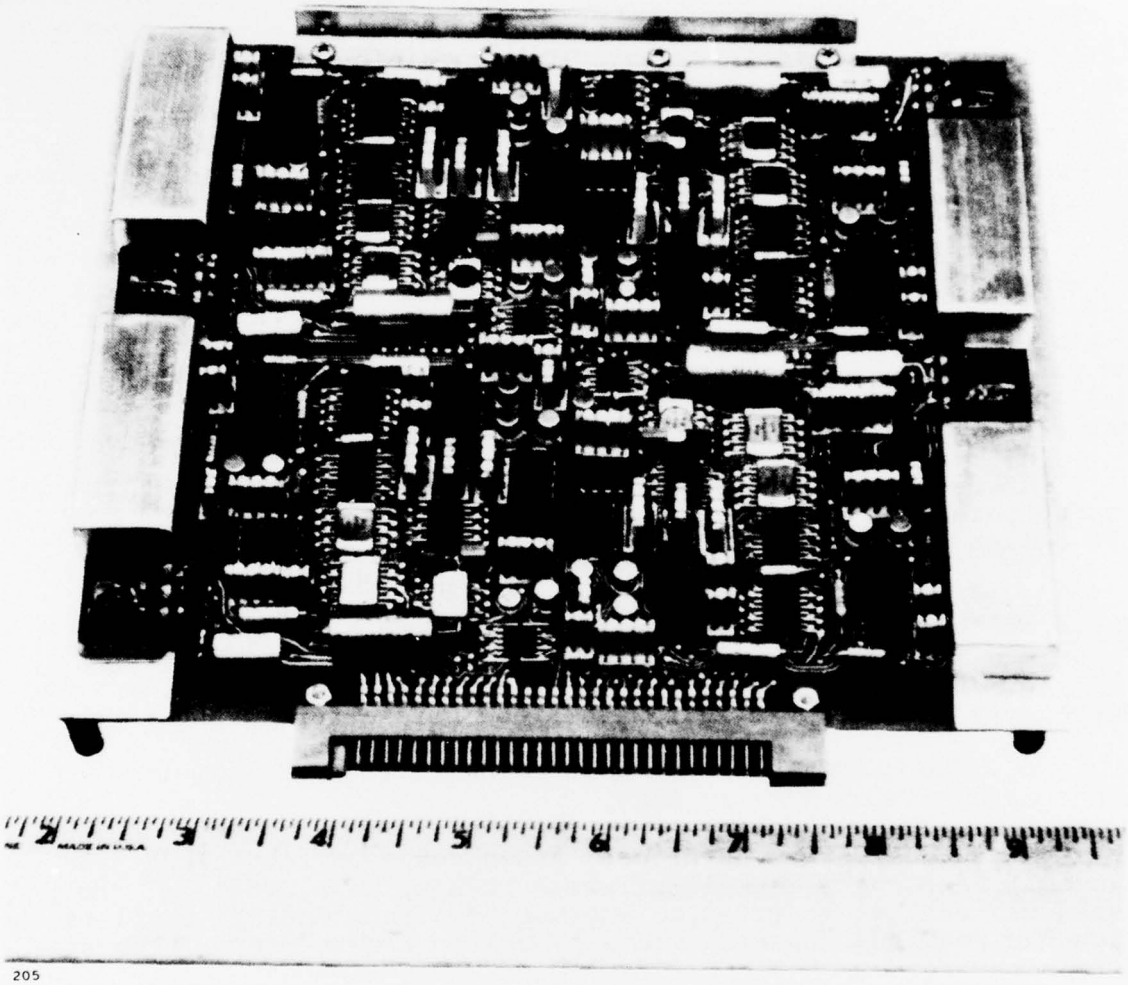


Figure 1. Power Controller Quad Card

	FAILURE EFFECT	PROBABILITY OF OCCURRENCE
3)	No significant change in power controller performance, but possible power controller failure on high load currents.	0.1870
4)	Increased power dissipation or DC offset voltage in power controller.	0.1854
5)	Failure of one or more of the following functions causing the controller failure.	0.5280
	a. Quick Trip Generator.	
	b. Time Trip Generator.	
	c. Zero Current Sensor.	
	d. Zero Voltage Sensor.	
	e. Pass element drive and control logic.	
6)	No immediate effect.	0.0102
7)	Loss of control signal to turn power controller ON.	0.0958
8)	Loss of Trip indication.	0.0309
9)	Power controller is always turned on irrespective of control signal.	0.0457

CONTROLLER FAILURE RATE = $8.2924F/10^6$ HRS.

MTBF = 120,592 HOURS

2.2.2 RELIABILITY PREDICTION

COMPONENT TYPE	FAILURE RATE 110^6 HOURS	FAILURE MODE	FAILURE EFFECT
TRANSISTORS	2.3066	75% SHORT	5C,2
DIODES	.9588	SHORT	1,6,7, 2,5E

COMPONENT TYPE	FAILURE RATE 110^6 HOURS	FAILURE MODE	FAILURE EFFECT
RESISTORS	.1743	OPEN	5B,5E,1, 6,3,7,5A
CAPACITORS	.0057	SHORT	5A,5B,5E, 1
INTEGRATED CIRCUITS	3.4110	OPEN	1 thru 9
OPTO-COUPLERS	.5000	OPEN	7,8
TRANSFORMER	.0560	SHORT	1
SOLDER POINTS	.8800		1 thru 9

TOTAL = 8.2924

2.3.0 TREE ANALYSIS SUMMARY

This section summarizes the results of the hardness assessment analysis of the Solid State Power Controller, for conformance to the B-1 neutron and prompt gamma radiation requirements. Specific details of this analysis is classified and was included in the interim report.

A neutron failure mode analysis was made of the Power Controller circuit elements. This analysis was performed by inspection of each element to determine their responses in the specified nuclear environments, based on available data as indicated in the references. Where data was inconclusive or not directly correlated to our environments, actual testing was performed.

Testing at the part level was performed by Northrup Radiation Facility. Testing at the specified neutron level was performed by Sandia on the complete power controller. The resulting degradation did not significantly affect their performance in the application.

An analysis of prompt gamma effects was performed by inspection and comparison of the subject devices to previously tested devices.

The normal circuit function of each major element was reviewed to predict its vulnerability to the prompt gamma pulse specified. Previous test data as indicated in the listed references has been used to the fullest extent possible. Testing was performed in areas where previous test data was insufficient.

Neutron degradation analysis, gamma dose rate and total gamma dose analysis have been performed on all circuit elements, with the degree of vulnerability determined. Results of these efforts show that the SSPC is sufficiently hard to meet B-1 specified radiation levels.

SECTION III

PROTOTYPE DESIGN AND TESTING PHASE

3.1.0 MECHANICAL DESIGN

3.1.1 SUMMARY

The mechanical design of the power control (Fig. 2) is predicated upon producing a unit that is small in size and weight, that can be readily produced in high volume at minimum cost and will perform reliably while subjected to the severest combinations of the specified environments for the duration of its intended service life. The design described herein is devised to accomplish these objectives by the use of techniques and materials that have been successfully tried and proved in quantity production of aerospace equipment by Telephonics and the aerospace industry.

3.1.2 ASSEMBLY

The mechanical components of the power controller, illustrated in figures 3 and 4 consist of the following:

a. Base plate on which are mounted the heat dissipative components.

b. Printed circuit board, which mounts the power supply components.

c. Connector board, which interconnects the pass and driver section with the flex print.

d. Flex print, a flexible printed circuit which mounts all other components and makes all interconnections.

e. Seamless drawn cover, which seals to the base and connectors.

f. The I/O connector, which interconnects the power controller with the aircraft.

g. Mounting screws, which fasten the power controller to the aircraft structure.

3.1.3 MATERIALS, PROCESSES AND FINISHES

All materials, processes and finishes are in compliance with specific MIL specifications or general MIL standards and have been used extensively by Telephonics in aerospace equipment.

Figure 2. Power Controller Can

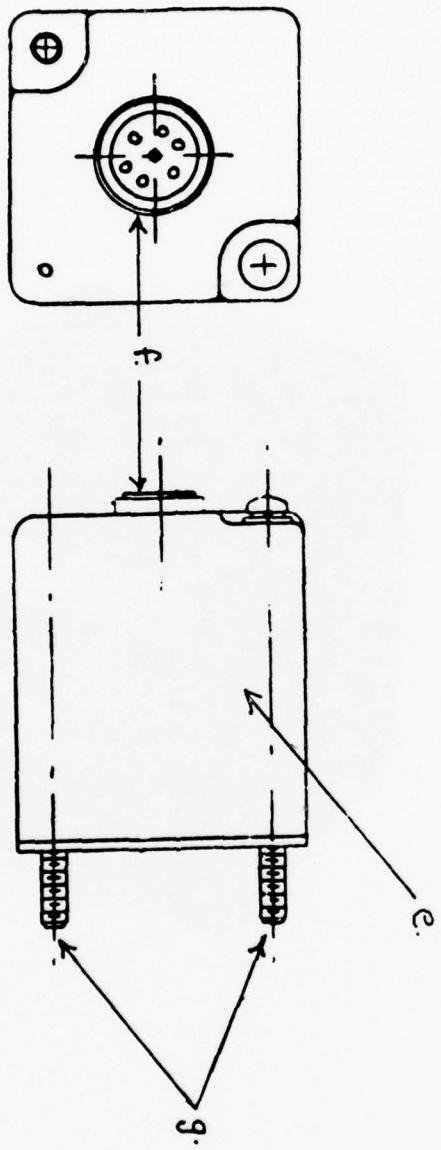


Figure 3. Power Controller Assembly Detail 1

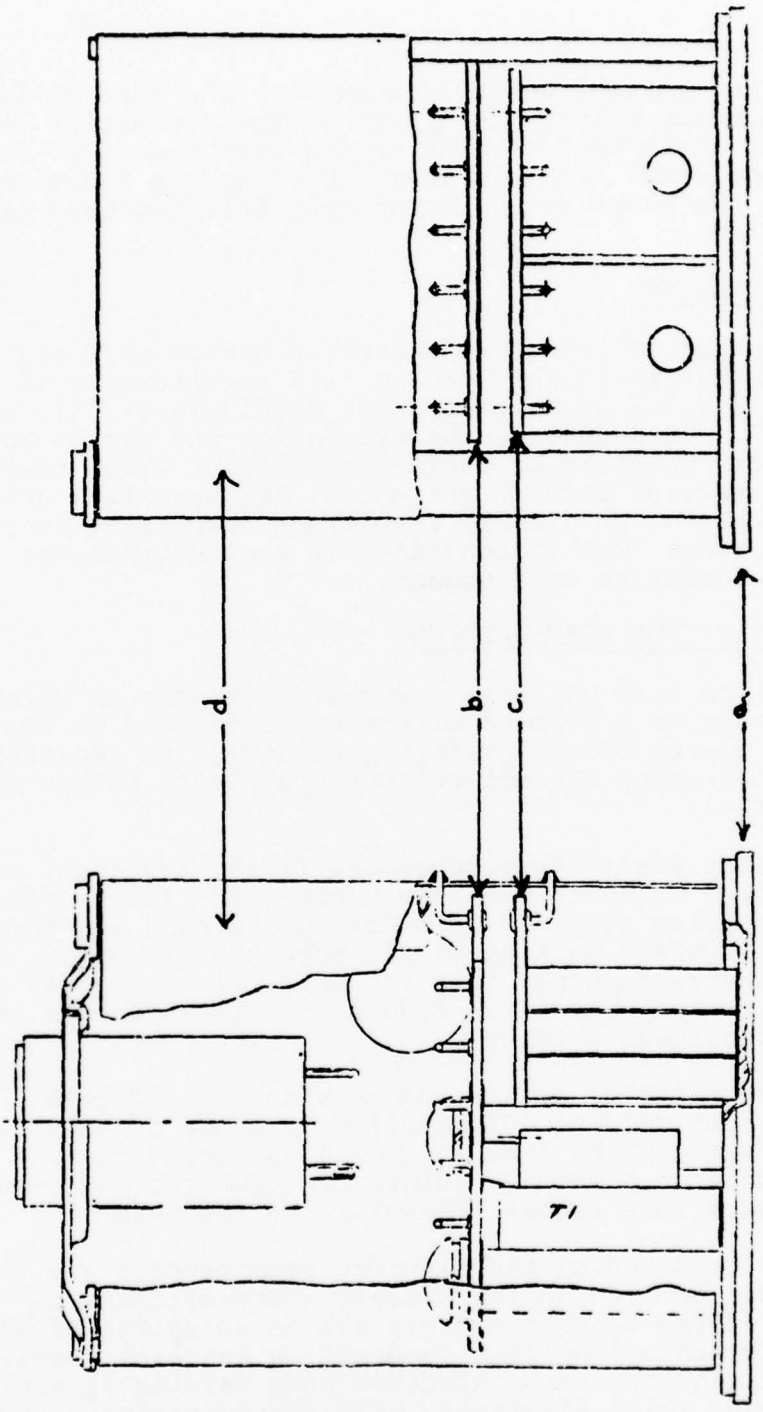


Figure 4. Power Controller Assembly Detail 2

For the initial delivery quantity, the base is fabricated from 5052-H34 aluminum alloy. For large volume production it can be molded from A356 by investment casting or die cast from A360 alloy. The cover is deep drawn from aluminum 1100-0 and is 0.019 thick. In production, the cover can be drawn from 6061 and heat treated to full hard condition.

3.1.4 SEALING

The assembly procedure described herein produces a hermetically sealed unit that meets the leakage rate requirements of paragraphs 3.2.3.3 and 3.2.3.7 of specification F33615-74-C-2031, attachment No. 1, Appendix "A". In addition, the evacuation and refil procedure eliminates any air, moisture or outgas contaminant which could affect performance or service life of the unit. All materials used are, in their final cured state, physically stable and chemically inert over a temperature range that is considerably greater than the specified storage and operation environments.

3.1.5 ELECTRON BEAM WELDING

Electron beam welding is a fusion process in which a dense high velocity stream or a beam of electrons is focused on the work piece. The kinetic energy of the impinging electrons is transferred to the material, increasing the molecular energy level to the melting point of the material.

The most significant advantage is the low total energy input to the work piece. This is possible because the fusion penetration of the high power density electron beam does not depend on thermal conductivity or on surface melting as do conventional welding methods. Electrons penetrate deeply into the material, instantly generating a very narrow fusion zone which reduces the total energy input to 1/25 that of conventional welding.

A wide range of metals and combinations of metals can be joined by electron beam welding. This allows the use of materials best suited for design, without the limits imposed by less versatile joining methods. Since no electrode points are required, the most intricate joint configuration becomes accessible to the beam.

Welds produced by the electron beam process are the strongest bonds that can be made in the present state-of-the-art. The exact controlability of the welding process allows adjusting of welding parameters to achieve optimum penetration patterns, sealing qualities and specific requirements. Electron beam welding is performed in a near absolute vacuum which eliminates weld contamination and oxidation, and assures maximum weld zone purity.

The process for electron beam busion welding is accomplished in accordance with specification MIL-W-46132, NAVSHIPS 250-1500 and ASME NUCLEAR "NPT", and has been used to hermetically seal electronic assemblies on the F-14, F-15 and "LEM" programs as well as for relays and electronic components.

Two difficulties were observed with respect to electron beam welding of the can:

a. Welding of the posts to the case body.

b. The unsoldering and displacement of the CTJ connector.

The combined effect of the anodizing around posts and the lack of material at the points to be sealed, resulted in a cutting action rather than a weld.

The addition of a collar around the flexprint support posts was made to rectify this problem. These collars provide the material needed to obtain a hermetic seal during welding. The unsoldering of the connector was attributed to the proximity of the electron beam and the heat generated therein. Once unsoldered, stress from the I/O leads pushes the connector away from the can. A retainer ring was incorporated around the connector body. Added prior to welding, the ring insured mechanical fastening of the connector to the case. In the event that sufficient heat was created to melt the soldered joint, the retainer ring absorbed the stress, preventing any displacement.

3.1.6 HEAT TRANSFER

Thermal design of the power controller is based on direct conduction to the heat sink upon which it is mounted. The components which dissipate 100 mw or more are conductively bonded to the base, thereby minimizing thermal resistance and consequently temperature rise. The clamping force of the #6-32 mounting screws, when tightened to the moderate dry torque of 15 in-lbs, results in an average contact pressure of over 300 PSI. The design of the base structure is devised to produce a dimensionally stable, flat, conductive interface of better than 63 micro-inch RMS roughness. The resulting contact resistivity will be less than $1^{o}C/Watt/in^{2}$ and in consideration of the net contact area of 2.6 in^{2} and a total dissipation of 4 watts, the average internal temperature rise will be less than $2^{o}C$. No difficulty is therefore anticipated in meeting the $3^{o}C$ rise limitations specified in paragraph 3.2.3.4 (Appendix).

The temperature rise of individual components above the internal average rise is likewise moderate. The highest dissipation occurs in the pass and driver transistor elements, which in their installed condition have a junction-to-base thermal resistance of not more than 1.2°C/Watt. The resultant temperature rise of these components is less than 1°C, for a total of less than 3°C above heat sink. Components mounted on the flexprint dissipate much less power, and although they will have much higher thermal resistances, their temperature rises do not approach levels that could affect their reliability.

3.1.7 ENVIRONMENTAL ENDURANCE

The environment which the power controller must endure can be classified into two categories: dynamic and natural.

The natural environment consists of the elements of temperature-altitude, humidity and salt fog, which could cause contamination and corrosion. Since the unit is inert internally and hermetically sealed, no internal effects can occur other than stresses induced by thermal expansion mismatch. The method used for seals and bonding of transistor elements is matched sufficiently close to the faying materials to preclude the possibility of failure within the range of thermal shock. All elements of the structure are aluminum and, therefore, compatible. Externally the surface is protected by paint.

The dynamic environment consists of shock, vibration, sustained acceleration and explosive decompression.

Explosive decompression subjects the walls and seals of the unit to an impulse pressure of 1045 psi/sec resulting from a differential of 10.45 psi occurring within 10 milliseconds. This pressure pulse is manifested in deflection of wall panels of the cover and consequent stress on the seals. The wall panels can be considered thin membranes subjected to diaphragm stress rather than plates in bending because of the large ratio of span to thickness. The combined tensile stress on the wall panels and from bending at the corners is small, in the range of 5,000 PSI as determined from equations and criteria given in MIL-HDBK-5A and "Analysis and Design of Flight Vehicle Structures" by E.J. Bruhn. The resultant shear stress which occurs on the joints at the base is within the bonding strength of the joint and does not result in creep because of the short duration.

A review of the specified shock, vibration and acceleration environment reveals that the destructive effects of vibration far exceed that of shock and acceleration. The cyclic repetition of vibration, considering both sinusoidal and random, transmits and

amplifies input displacements throughout the unit to a degree that is greater than that which is induced by a comparatively few shock pulses and the kinetic transfer from sustained acceleration. The endurance limit effect of vibration is, therefore, the primary concern in the design of the Power Controller structure and support of the internal electronics.

The fundamental consideration in designing for a vibration environment is resonance of the basic structure. The objective is to produce the highest practical natural frequency so that resonant amplifications will not cause large displacements, therby endurance limit failures can be avoided. The basic equation for determining natural frequency of a simple structure is:

$$f_n = \frac{1}{2}\sqrt{\frac{k}{m}}$$

where k = spring rate = $\frac{P}{\delta}$ (load) / (static deflection)

m = supported mass

The basic structure can be considered a cantilever, and to be conservative the load is considered to be concentrated at the end, therefore:

$$\delta = \frac{P\ l^3}{3\ EI}$$

where:

P = load - lbs
l = span - in
E = modulus of elasticity
I = section moment of inertia
δ = static deflection

Substituting the appropriate values for 0.019 gauge aluminum, .253 lbs weight, 1.625" square section and 2.10" length, the static deflection is 1.4704×10^{-6} inches and f_n = 2704 Hz.

In sinusoidal vibration per MIL-STD-810 method 514.1 procedure II part 1, the frequency range is 50 to 2000 Hz and the maximum intensity is 15 g's. Assuming a conservative transmissibility of 10, the displacement of the structure is 1.6×10^{-4} inches double amplitude. This is a very safe level of response, even when a 30 minute resonance dwell is considered.

The random vibration spectrum, as specified in part 3 of procedure II, method 514.1 reaches a maximum intensity of .7 g^2/Hz in the frequency range of 100 to 1000 Hz with a 6 db/oct ocrease from 50 Hz and a 6 db/oct decrease from 1000 to 2000 Hz. Using the following equations, the equivalent grms values for a one-sigma distribution can be determined:

a. $g^2 = \frac{3w}{3+m}\left[f_2 - f_1 \quad \frac{f1}{f2} \quad {}^{m/3}\right]$

b. $g^2 = w\,(f_2 - f_1)$

c. $grms = \sqrt{g_1^2 + g_2^2 + g_3^2}$

where w = intensity g^2/Hz

m = change rate in db/oct

f_2 = higher frequency Hz

f_1 = lower frequency Hz

$grms = \sqrt{45.19 + 560 + 262.5} = \underline{29.456}$

This level of equivalent intensity is not severe when two aspects are considered:

a. All frequencies and displacements are distributed according to a Gaussian curve, no resonance dwell occurs, and the instantaneous effect of any resonance is reduced by side band interference.

b. The maximum single amplitude displacement at resonance is only 8×10^{-6} inches at a power spectra density of .09 9^3/Hz, therefore, the resulting stress levels will be below the endurance limit design margins.

The transmission of vibration from the structure into the flexprint is small considering the pliable nature of the material and the attenuation effects of the conformal coating. The flexprint responds much lower frequencies than the structure, with considerably larger displacements. However, when the inherently rugged nature of solid state miniature components and the reinforcement of the coating are considered, the possibility of failure is small.

3.1.8 WEIGHTS

A major consideration in formulating the design concept of the power controller has been minimum weight. The following table is a summary and detailed breakdown of the elemental weights. During the course of the development program close surveillance was maintained to trim weight wherever feasible.

SUMMARY OF COMPONENT WEIGHTS

	WT IN GRAMS
Flex Print Components	21.97
Flex Print With 0.015 thick Backup	7.60
Case	13.00
Posts (2)	.55
Base	12.00
Connector	13.87
Extension Screws (2)	3.42
Screws (2)	8.58
Connector Support	1.00
Conformal Coating	4.32
Transformers	8.10
Printed Circuit Board	2.00
Pass & Driver Transistor Connector Board	1.16
Power Supply Components	10.90
Hardwire	.60
Kapton Film	.60
Steel Shield Assembly	5.13
	114.80 Grams
	4.05 oz.
	.253 lbs

3.2.0 ELECTRICAL TESTS

3.2.1 SUMMARY

Every electrical test called for the design specification has been performed successfully, at -55°, 25° and 75°C. A typical lab

data sheet used is shown in figure 5. On the following pages typical waveforms are shown and discussed, revealing the performance of the SSPC during the testing of critical parameters.

Data sheets for the Qualification Test units are contained in a separate report.

Figure 6 shows some of the specialized test equipment that was used in the development and testing of the SSPC.

3.2.2 LOAD COMPATIBILITY

To insure the compatibility of the SSPC with the wide variety of loads found on the B-1 aircraft, a comprehensive test program included capacitive, inductive, nonlinear, motor, transformer and half wave resistive loads connected to the power controller. The photographs in figures 7 through 11 demonstrate the CLEAN "0" voltage turn on, "0" current turn off feature of the SSPC which eliminates the UNDESIRE-ABLE contact bounce and arcing found in most electro-mechanical relays.

Problems encountered in the development of the SSPC with respect to load compatibility were primarily confined to three areas:

a. Capacitive loading beyond the specified .9 power factor.

b. Light inductive loads (<1MH) present during rupture testing.

c. Light resistive loading (>10K) at -55°C.

Capacitive loading (as evident in figure 11) has the effect of holding a charged voltage at the power controller's output terminals. The voltage is present due to the SSPC "0" current turn off ability. At the time of turn-off the voltage remaining is a function of the phase relationship between current and voltage for the particular capacitance in the load. The voltage magnitude is inversily proportional to the power factor (e.g. as the load approaches a pure capacitance the remaining voltage approaches the peak line voltage). Since the input line voltage to the SSPC is continually present, the pass section will be subjected to periodic excursions of the sum of V line peak and V charge. At 0 power factor with a high line voltage present, V charge = 1.414 x 244 ≅ 345V V line peak + V charge = 2 x 345 = 690V. This voltage is within BV_{CEO} of the transistors utilized in the pass section.

Although this extreme condition is not within the specified limits of power controlled operation, much attention was paid in selection of a suitable pass element.

TEST	RESULTS AT 25°C	-55°C	75°C	SPEC. LIMITS
Turn on threshold voltage	2.91V	3.61V	2.55V	4V 2.1 to 3.9 volts don't care range
Turn off threshold voltage	2.89V	3.56V	2.51	2V
Turn on current when Vc = 6V	9 ma	9ma	9ma	10ma
Trip voltage, Isource = 2ma	0.475V	0.380V	0.645V	1V
Turn on delay time	10ms	6.5ms	10ms	5 - 15 ms
Turn off delay time	6ms	8ms	6ms	5 - 15 ms
Zero current turn off	10ma	10ma	19ma	±20ma
Zero voltage turn on	15ma	15ma	17ma	±20ma
Voltage drop at rated load	1.8V	2.1V	2V	2.3
Instant Trip	O.K	O.K	O.K	X
Output leakage (trip output circuit)	20μA	21μA	19μA	25μA
Time trip:				
200%	1.7 sec	1.4 sec	1.8 sec	0.35 - 2 sec
500%	140ms	138ms	150ms	0.05 - 0.35 sec
Open circuit turn off	X	X	X	No Damage
Input transients (360 Vrms to 140 Vrms)	X	X	X	" "
Half waving loads ± direction	X	X	X	" "
Capacitance Load	X	X	X	" "
Inductive Load	X	X	X	" "
Control Noise Immunity Test	X	X	X	" "
Control Input Transient Test	X	X	X	" "
Trip Output Circuit Transient Volt.	X	X	X	" "
Leakage Current	0.21ma	0.2ma	0.22ma	1ma
Peak let through current (with short circuit applied at peak voltage)	25A	24	20A	35A
Power Dissipation	X	X	X	Given Curve

Figure 5. SSPC Data Sheet

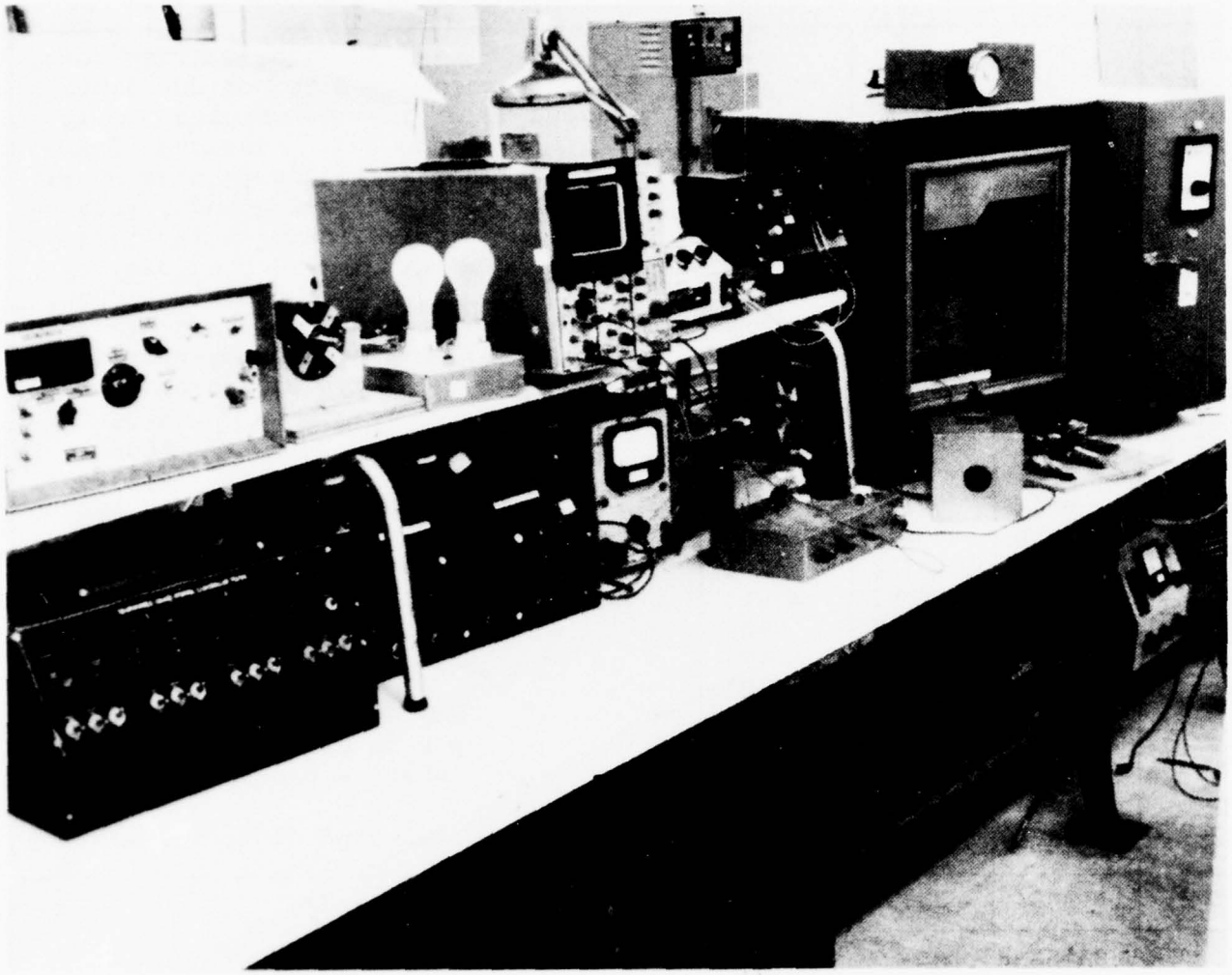
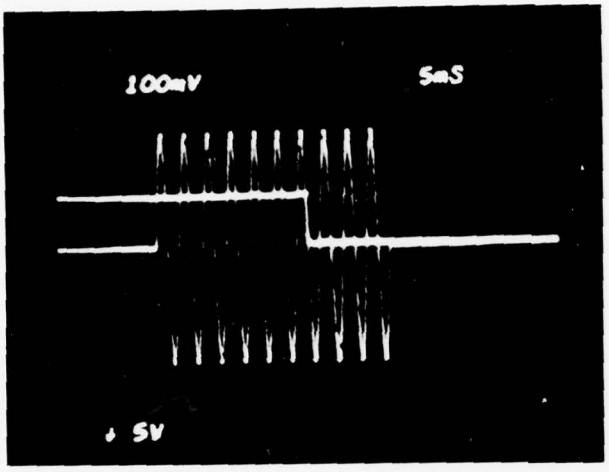


Figure 6. Test Set-Up

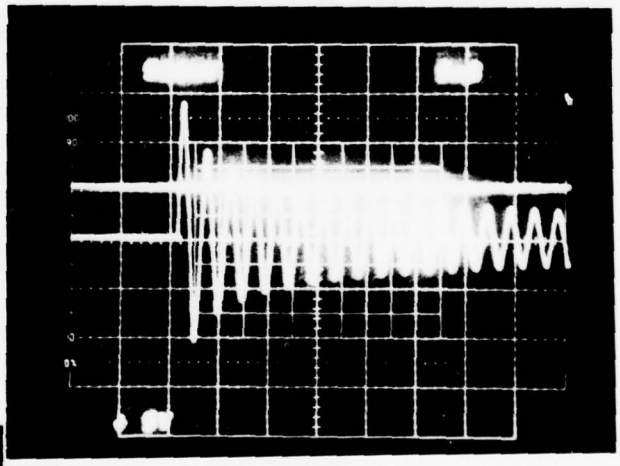


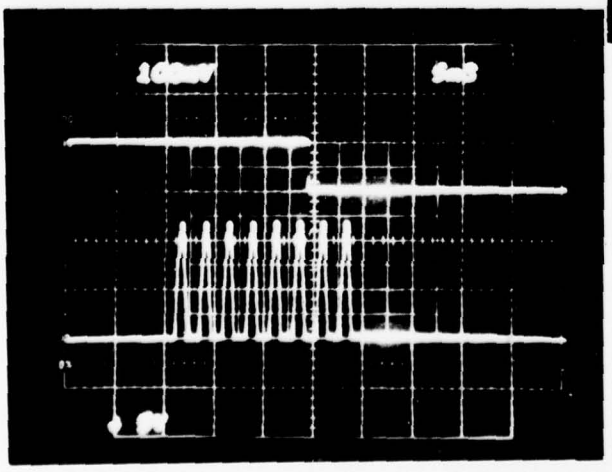
TURN ON AND OFF INTO
RATED LOAD. LOAD CURRENT
@ 1A/CM VS. CONTROL
VOLTAGE @ 5V/CM

Figure 7.

TURN ON INTO
NON-LINEAR LAMP
LOAD. LOAD CURRENT
@ 5A/CM VS. CONTROL
VOLTAGE

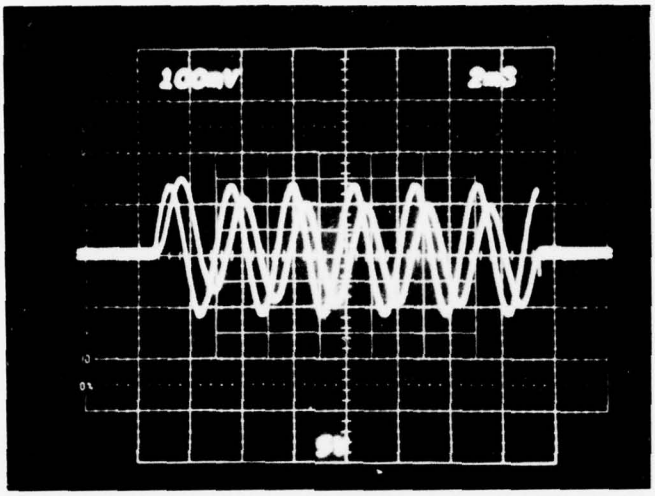
Figure 8.





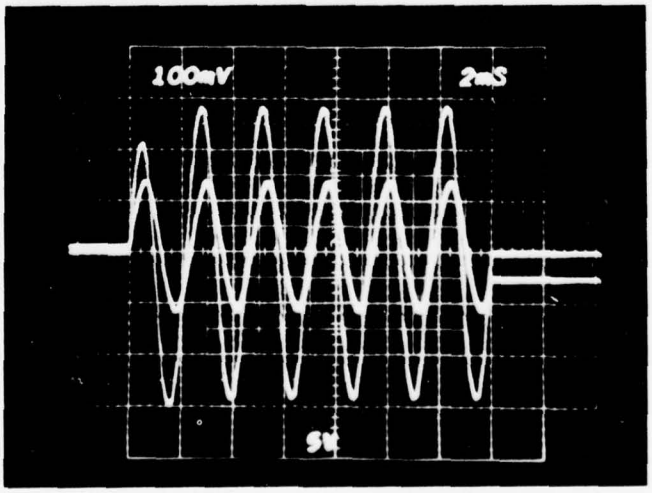
HALF WAVING LOAD
CONTROL VOLTAGE @ 5V/CM
VS. LOAD CURRENT @ 1A/CM

Figure 9.



INDUCTIVE LOAD P.F. = .3
COMPLETE ON/OFF CYCLE
LARGE SIGNAL = LOAD VOLTAGE @ 250 V/CM
SMALL SIGNAL = LOAD CURRENT @ 1A/CM

Figure 10.



CAPACITIVE LOAD P.F. = .9
COMPLETE ON/OFF CYCLE
LARGE SIGNAL = LOAD CURRENT @ 1A/CM
SMALL SIGNAL = LOAD VOLTAGE @ 250 V/CM

Figure 11.

Because of the applicability of light inductive loads as a problem area during rupture testing, they are discussed in paragraph 3.24 under the heading, Rupture Test and Instant Trip.

Light resistive loading @ -55°C was a minor problem which appeared early in the SSPC design effort. It was manifest by the frequent inability of the control logic to turn the pass element off. The problem was rectified by the addition of temperature compensating circuitry to the effected area.

3.2.3 OPERATING VOLTAGE TRANSIENTS AND PULSED LOAD

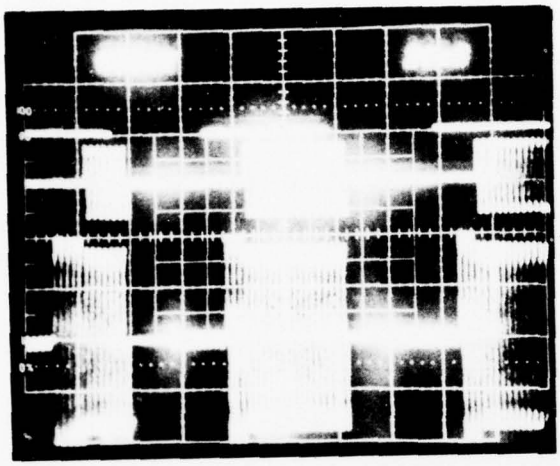
A more severe test than required by the general design specification was performed on the SSPC. By using two SSPC's in series from a variable 400 HZ source, we were able to initiate line voltage changes of 360 V. rms. and apply them to the unit under test i.e., the unit furthest from the source. Figures 12 through 18 indicate that the SSPC operates normally and within the requirements of the specification while exposed to these transient conditions. With maximum off control voltage the 400 Hz power input may be varied from 0 V. rms. to 360 rms. without changing the state of the SSPC. The same is true when the minimum of control voltage is applied.

By reversing the manner in which the control voltage is applied to the series connected SSPC's, it is possible to demonstrate the effect of a pulsed load. (Figure 19) In this photograph, a continuous control voltage is applied to the unit under test and a second power controller is connected in series with the load. The second SSPC is activated with the control signal shown in the upper trace. The lower trace is load current.

The relative ease which with these modes of operation may be demonstrated are indicative of the immunity transistors possess to large values of $\frac{\Delta V.}{\Delta T}$

3.2.4 INSTANT TRIP AND RUPTURE TEST

The distinct advantage of full cycle control of the transistorized pass element is evident when the power controller output is presented with a short. Full cycle control, in this context, means the ability of the power controller to turn power off at any phase within the 400 HZ cycle. Thus protecting the source and line from excessive currents. Under such conditions, load current is dependent on the intrinsic electrical parameters of three variables. The first of these variables is the power source. Deviations from an idealized power source to one encountered in actuality makes it difficult to predict load current, unless the source is fully characterized. This means that the line impedances over a wide frequency range must be known.

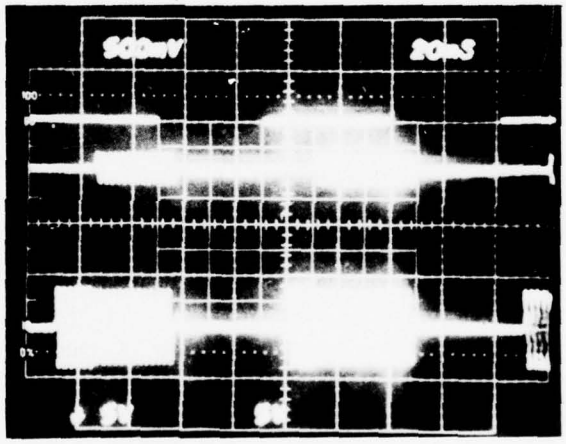


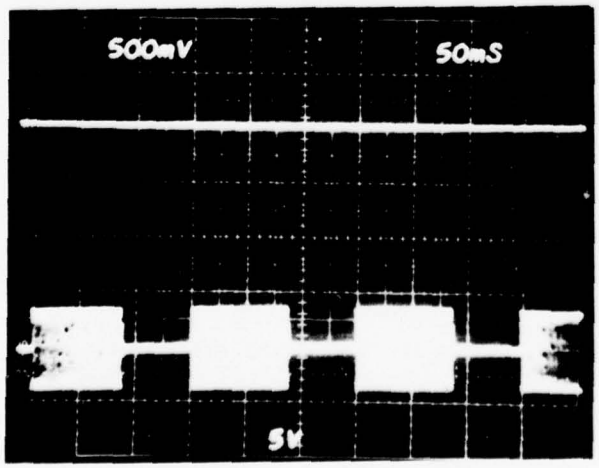
PULSE INPUT TRANSIENT
TWO SSPC'S IN SERIES UPPER
SIGNAL = CONTROL VOLTAGE
TO UNIT #1 (CLOSEST TO THE
SOURCE) @ 5 V/CM
MIDDLE TRACE = LOAD CURRENT
@ 5A/CM
LOWER TRACE = UNIT #1
OUTPUT @ 250 V/CM

Figure 12.

PULSED INPUT TRANSIENT
CONDITIONS THE SAME AS
FIG. EXCEPT THAT
SOURCE = 140 VRMS

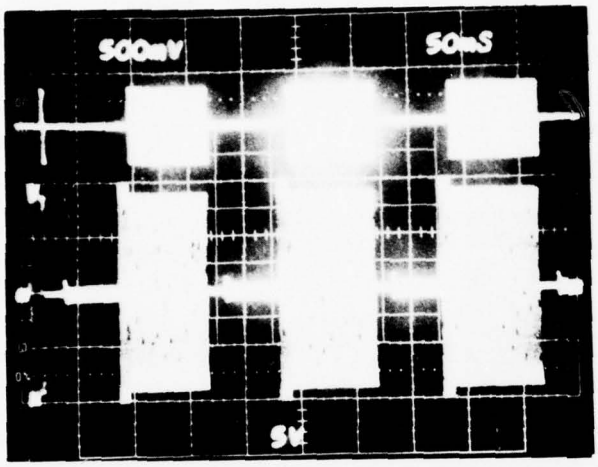
Figure 13.





PULSED INPUT TRANSIENT
UPPER TRACE = LOAD CURRENT
@ 5A/CM
LOWER TRACE = APPLIED
VOLTAGE @ 250 V/CM
CONTROL VOLTAGE SET TO MAXIMUM
OFF VALVE (2V)

Figure 14.

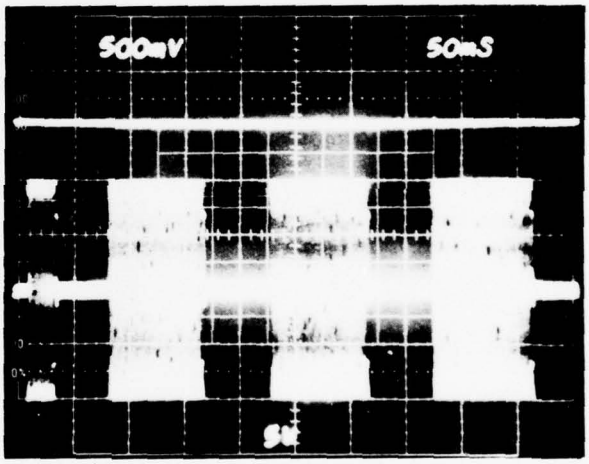


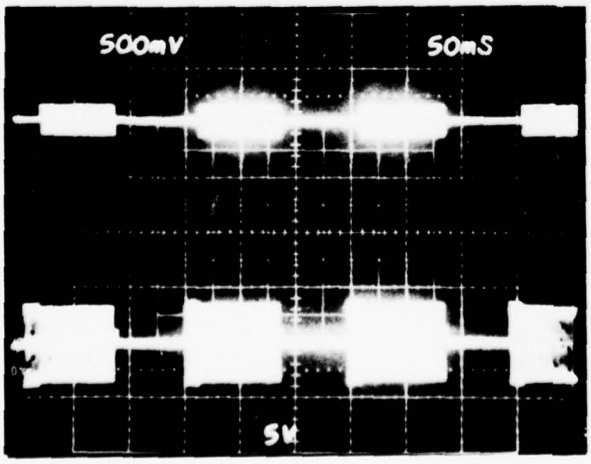
PULSED INPUT TRANSIENT
UPPER TRACE = LOAD CURRENT
FOLLOWING THE APPLIED 360 VRMS
TRANSIENT @ 5A/CM
LOWER TRACE = APPLIED VOLTAGE
@ 250 V/CM
CONTROL VOLTAGE SET TO
MINIMUM ON VALVE (4V)

Figure 15.

PULSED INPUT TRANSIENT
WITH CONTROL INPUT
VOLTAGE SET TO MAXIMUM
OFF VALVE (2V)
UPPER TRACE = LOAD CURRENT
@ 5A/CM
LOWER TRACE = APPLIED
VOLTAGE @ 250V/CM

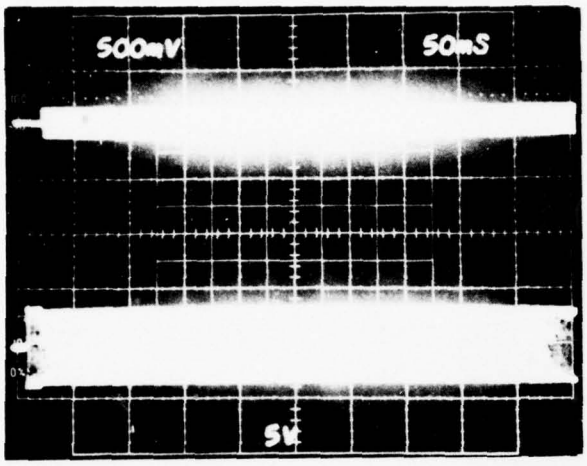
Figure 16.





PULSED INPUT TRANSIENT
@ 140 VRMS
UPPER TRACE = LOAD CURRENT
@ 5A/CM
LOWER TRACE = APPLIED
VOLTAGE @ 250 V/CM
CONTROL VOLTAGE SET TO
MINIMUM ON VALVE (4V)

Figure 17.

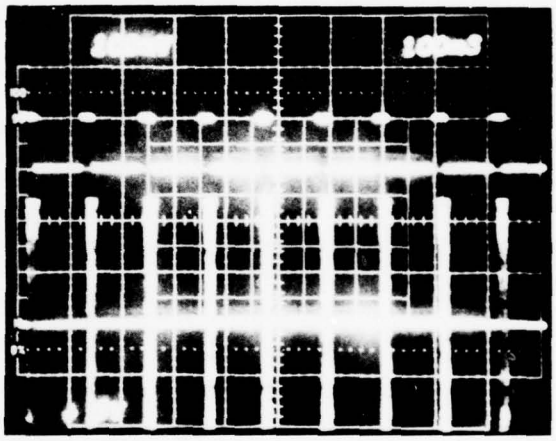


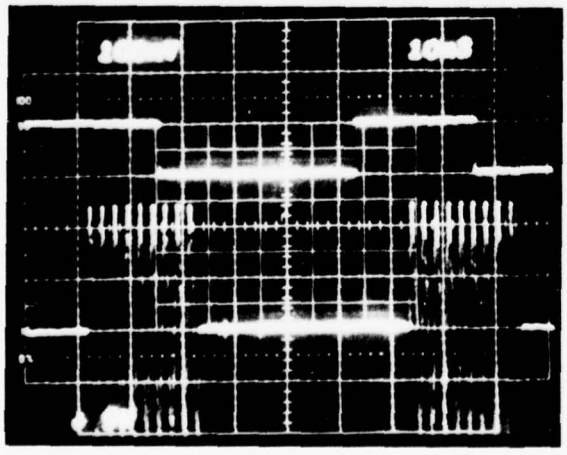
LOW LINE OPERATION @ 140 VRMS
UPPER TRACE = LOAD CURRENT
@ 5A/CM
LOWER TRACE = APPLIED VOLTAGE
@ 250 V/CM

Figure 18.

PULSED LOAD OPERATION
TWO SSPC IN SERIES
P.C. #1 (CLOSEST TO SOURCE)
SUPPLIED WITH CONTINUOUS
ON SIGNAL.
UPPER TRACE = CONTROL
VOLTAGE APPLIED TO P.C.
#2 @ 5 V/CM
LOWER TRACE = LOAD CURRENT
@ 1A/CM

Figure 19.





PULSED LOAD
EXPANDED VIEW OF FIGURE 19

Figure 20.

The above impedances are determined by 3 elements; by the 400 HZ generator output impedance, by the 400 HZ transmission line from the generator to the load and power controller and by the line transformer with taps for the desired line voltages. Data on the above elements are usually available for the power frequency, i.e. 400 HZ. However, the switching phenomena triggered by the power controller contain rather high frequencies that lie, usually, in the range of 100 KHZ to 1 MHZ. To obtain data for these frequencies special measurements were carried out that produced the necessary output impedances of the generator, the transmission line and the line transformer.

The results of the above measurements are shown in figures 21 and 22. Figures 21 and 22 represent the Telephonics in house generator and line transformer output impedances respectively. These data and estimated data for transmission line were then reduced to equivalent circuits with lumped constants. Figure 23 presents an equivalent of the 400 Hz line.

The second variable considered was the power controller pass element. Peak load current and waveshape are a function of the dynamic impedance of the pass section and the manner in which it is controlled. Events that occur during the interval of the applied short are also governed to a large extent by the particular device chosen for the pass element. Subsequently, much of the detailed testing outlined in the interim report was done to satisfy the requirements of this mode of operation.

The last variable considered was the load. In this case, load current was primarily a function of the phase of the 400 HZ cycle at which the short was applied. Two probable short circuit failure modes were defined as Instant trip and Rupture test. In Instant trip the power controller under test is turned on into a shorted load. Due to the zero voltage turn-on capability of the power controller, load current rises as the line voltage begins its positive going zero crossing. When the load current exceeds 1000% of rated load the pass section turns off. In Rupture test the power controller is on and delivering the rated load current (1.6A) when the short is applied. The short is selected to occur at either the positive or negative peak of the line voltage, as shown in figure 24. Load current rises rapidly during the test, subjecting the power controller to a worst case failure mode.

The following experimental observations have been made to expand upon some of more generalized statements made thus far. Figures 25 and 26 are typical current waveforms during Rupture test. Figure 25 is a positive rupture and figure 26 is negative. Current magnitude is 10A/cm @ 20 usec/DIV. Total inductance in the line estimated by the initial slope = E peak $\frac{\Delta T}{\Delta I}$ = 230 X 1.414 X $\frac{6 \times 10^{-6}}{15}$ = 130uh.

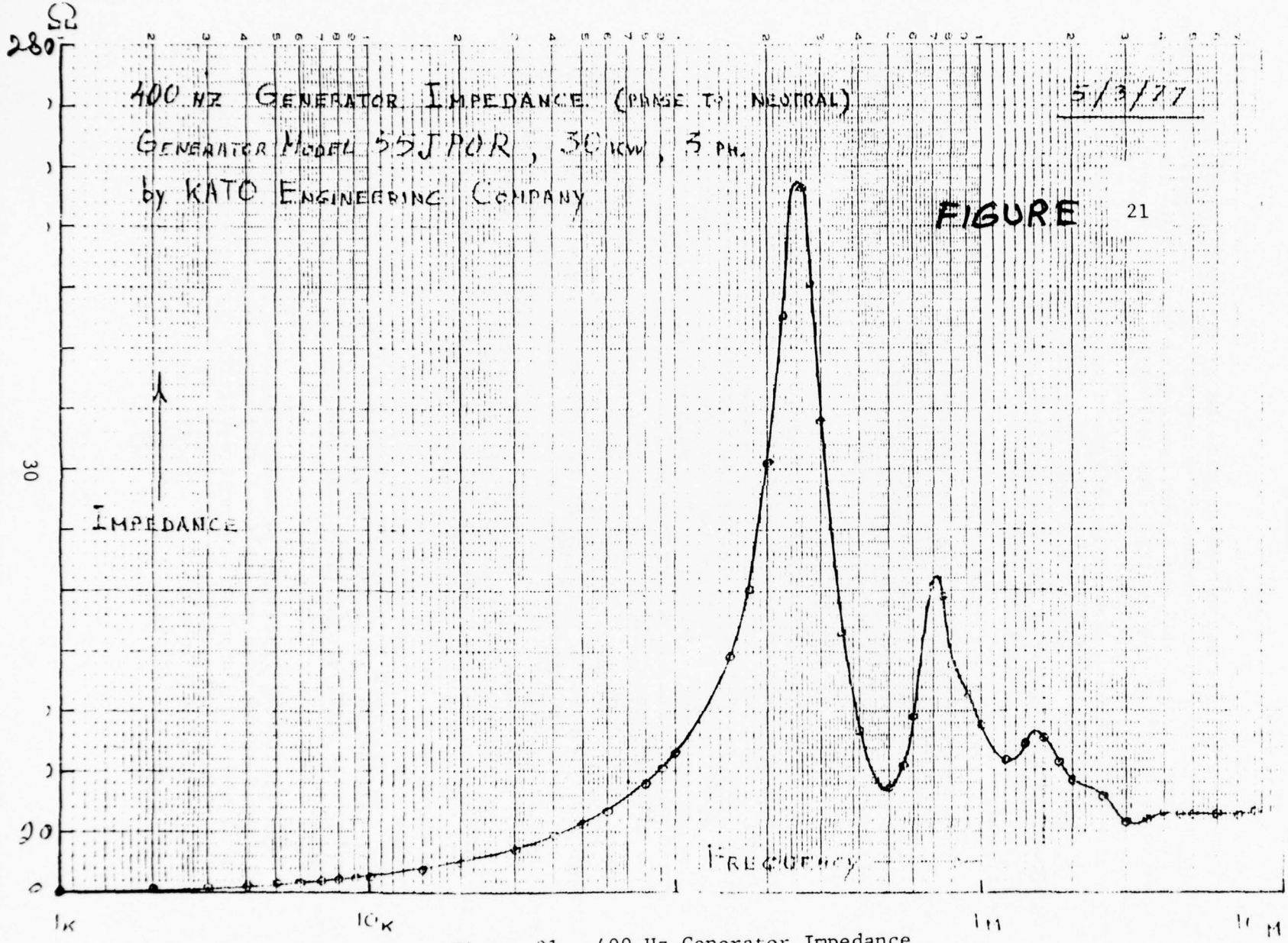
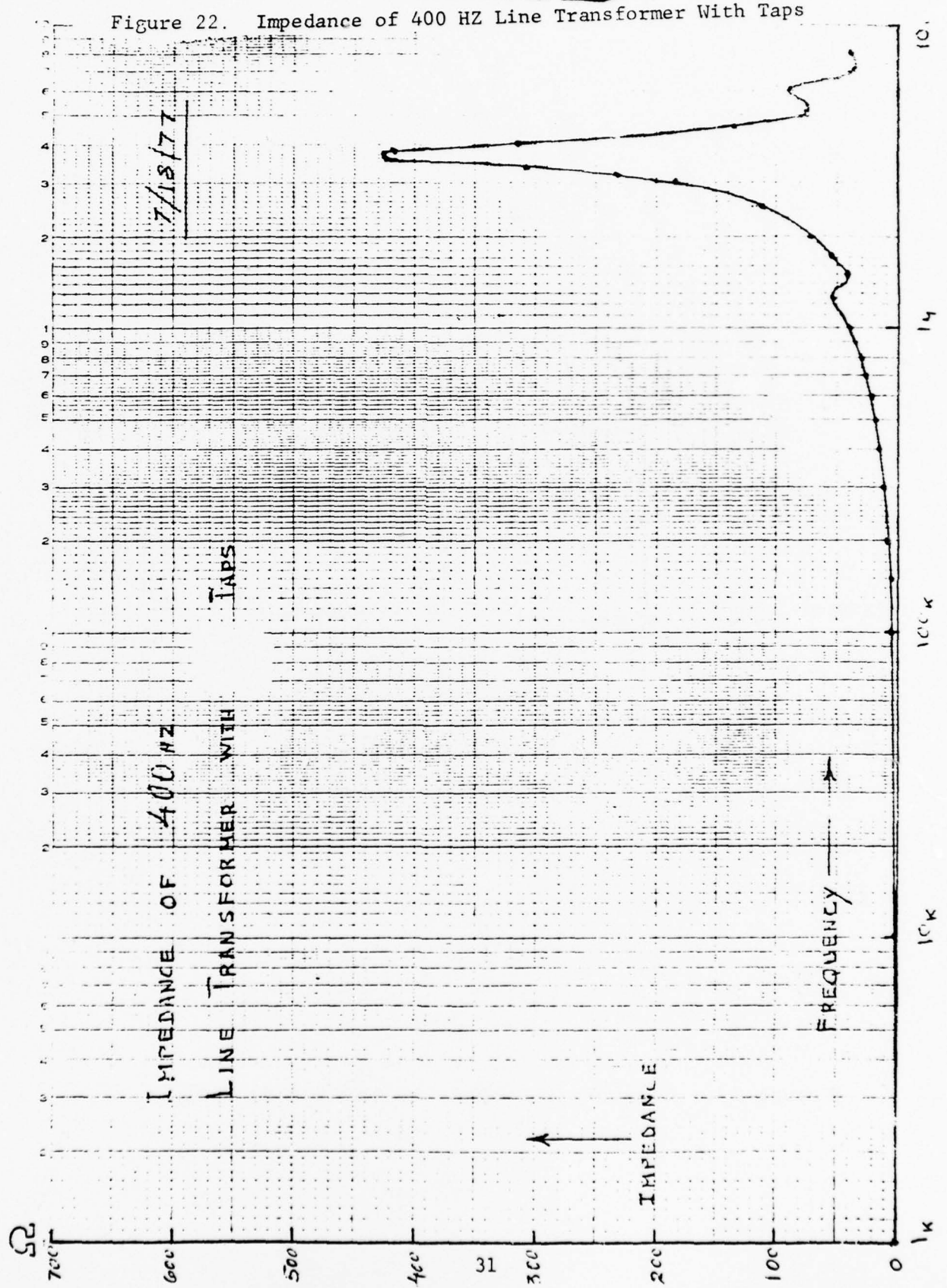


Figure 21. 400 Hz Generator Impedance

Figure 22. Impedance of 400 HZ Line Transformer With Taps



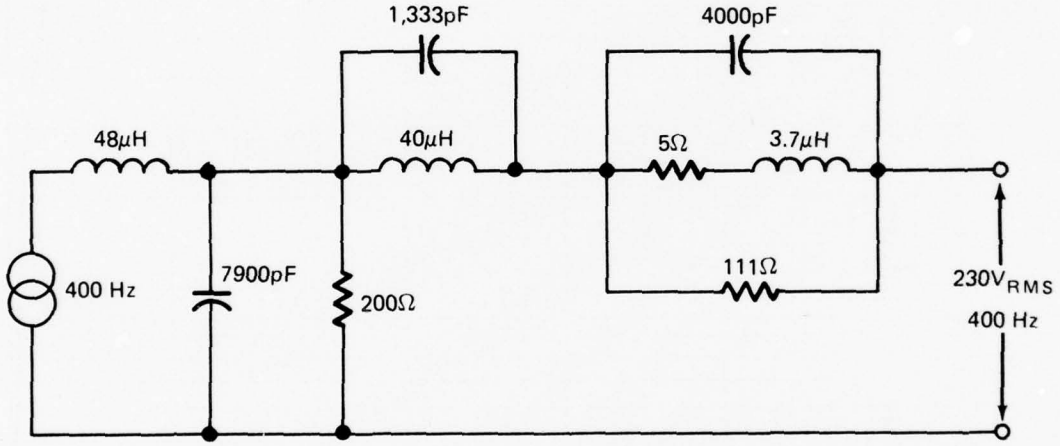


Figure 23. Equivalent Circuit of the 400 Hz Line

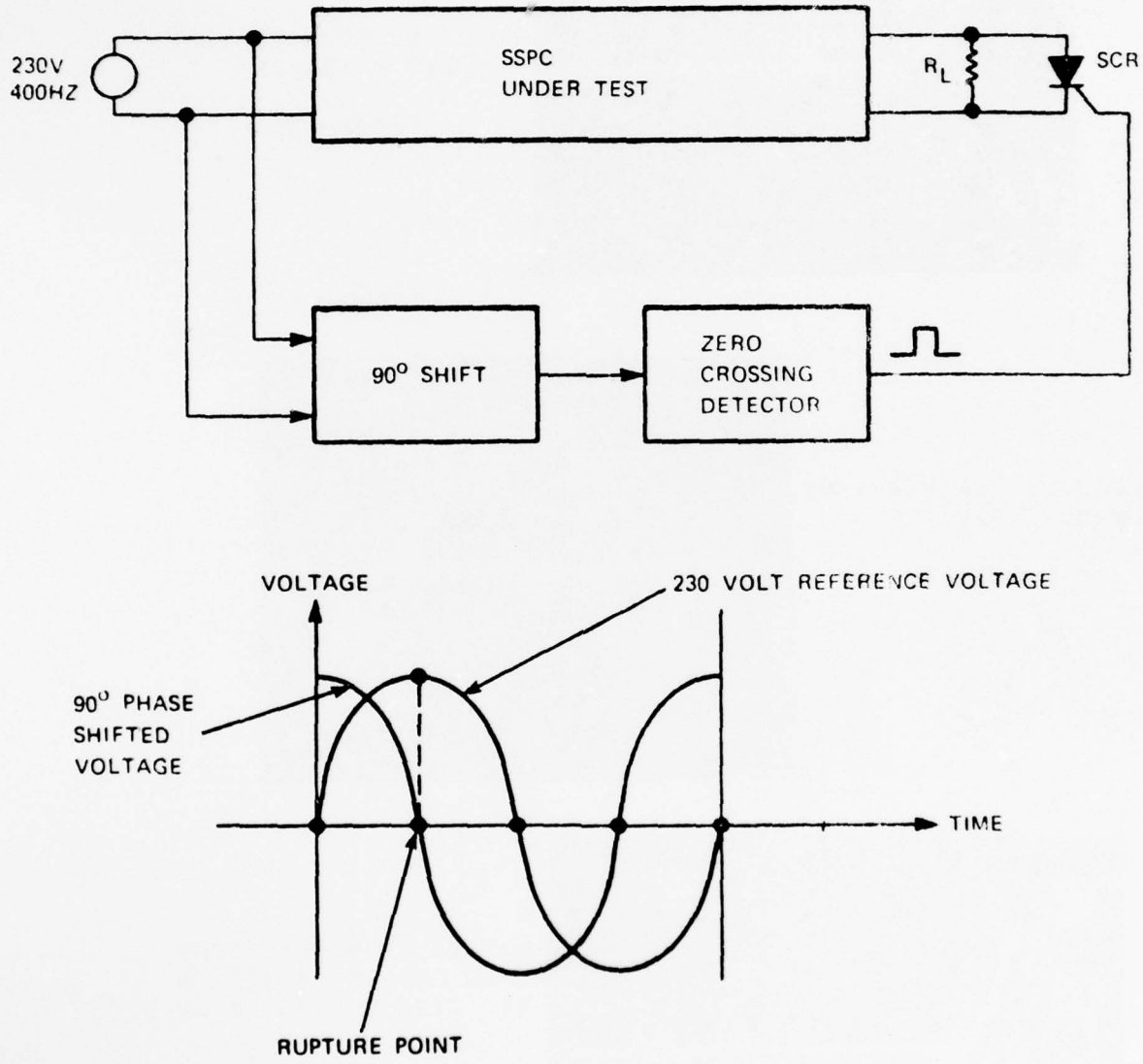
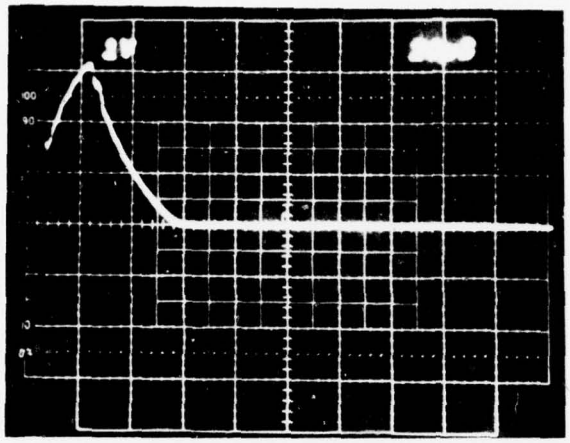
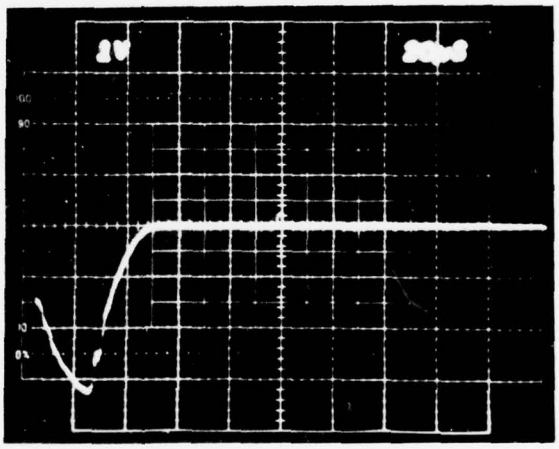


Figure 24. Rupture Test



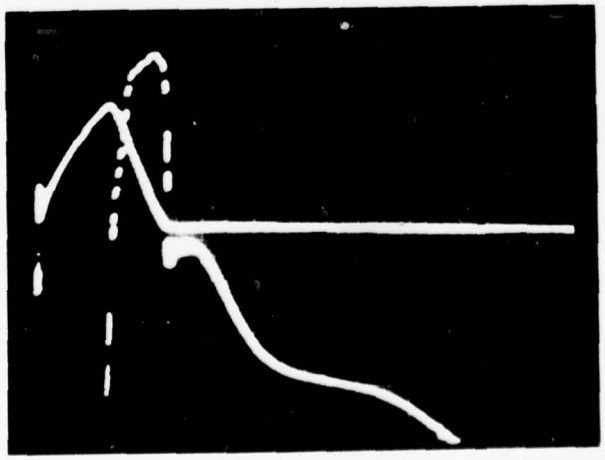
POSITIVE RUPTURE TEST
CURRENT = 10A/CM

Figure 25.



NEGATIVE RUPTURE TEST
CURRENT = 10A/CM

Figure 26.



POSITIVE RUPTURE TEST
LOAD CURRENT @ 10A/CM
VS. LINE VOLTAGE @ 50 V/CM

Figure 27.

A small discontinuity is noticeable in each figure @ 4 usec after the current has reached its peak value. The discontinuity is noteworthy when the line voltage at the power controller's input terminals is also viewed (Figure 27). In this figure, it is evident that the discontinuity represents the time in which the line inductance is transferring stored energy $\left(\frac{LI^2}{2}\right)$ to the pass element. This energy is manifest as a voltage spike in series with the line voltage. Since the line voltage is the same voltage that appears across the pass element at the time of the short, the product of E x I x T is the energy that must be absorbed. The total energy is given by equation

$$\left(E_{S/B} = \frac{LIc_{(MAX)}^2}{2} \left[1 - \frac{\frac{1}{Vcc}}{Vce(SUS)} \right] \right)$$

which also accounts for the energy drawn from the power source. In this case the energy = 100mj. During this time the pass transistors are operating in the sustaining mode with the peak line voltage, (@520V) being the VCEsus.

Figure 28 shows the effect of swamping out the line inductance by the addition of a 10 mfd capacitor. It's shown that the current reaches a higher peak value in a shorter period of time. In addition, the line voltage spike is evident to a lesser degree due to the small stray inductance in the power controller current loop.

Figure 29 is the current waveform during instant trip. It is interesting to note that the time taken for the current to reach its peak value is long compared to the rupture test. This is due to low Vce and BETA across the pass element when the power controller is turned on. Similarly, placing a capacitor across the input line has negligible effect on peak-let-thru current.

3.2.5 CONTROL INPUT TRANSIENTS

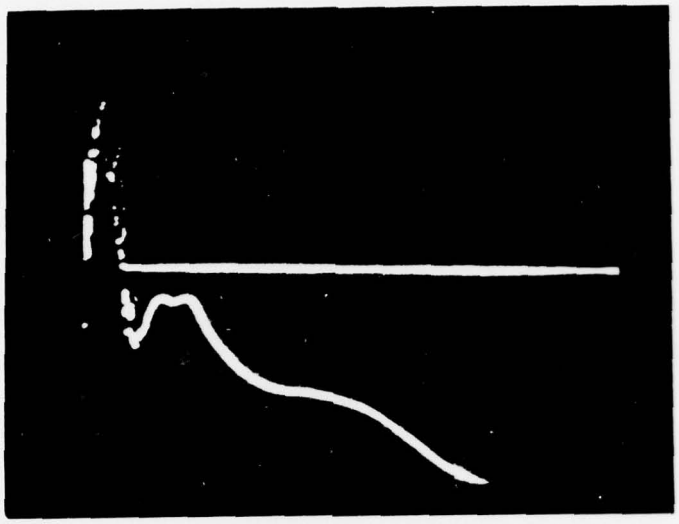
The transient generator used provided $\pm$ 100 volt peak signals from an output impedance of 250 ohms. The lower traces in Figures 30 and 31 represent output current at 0 amps. Note that the SSPC is immune to this type of transient.

3.2.6 "O" VOLTAGE ON, "O" CURRENT OFF

Figure 32 is a blown up view of the load current into a rated resistive load in compliance with specified parameters.

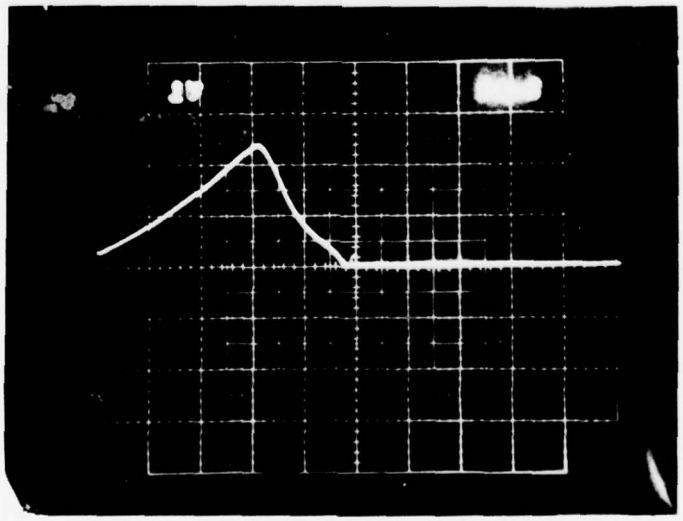
3.2.7 TIME TRIP

Figures 33 and 34 reveal that applying a 200% and 500% overload to the SSPC causes the unit to trip within the required time.



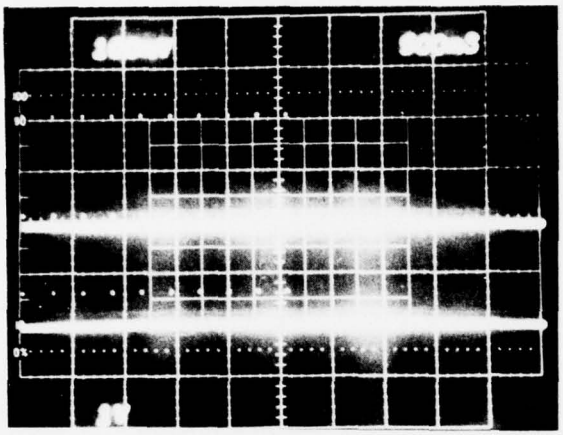
POSITIVE RUPTURE TEST
LOAD CURRENT @ 20A/CM
VS. LINE VOLTAGE @ 50 V/CM

Figure 28.



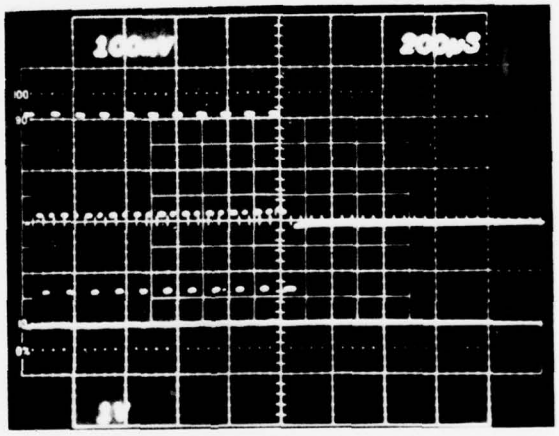
INSTANT TRIP
LOAD CURRENT = 10A/CM

Figure 29.



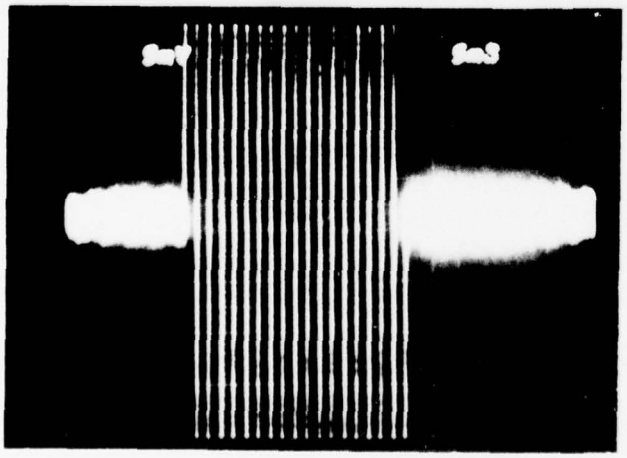
CONTROL INPUT TRANSIENT
ONE OF 10 BURSTS FROM
± 100V PEAK GENERATOR
SIGNAL = 10 V/CM
LOWER TRACE = LOAD CURRENT
@ 1A/CM

Figure 30.



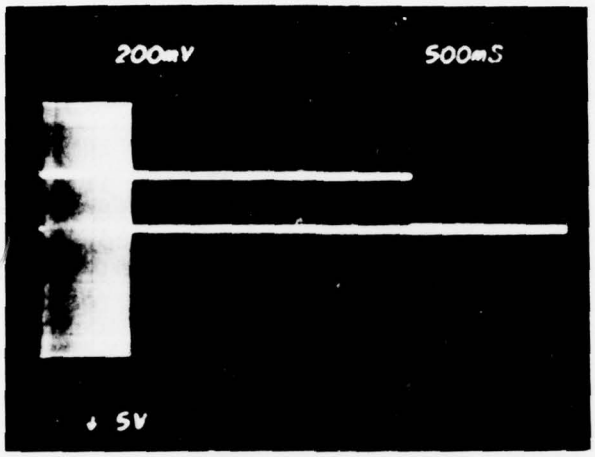
EXPANDED VIEW OF ONE
BURST OF FIG. 3-29

Figure 31.



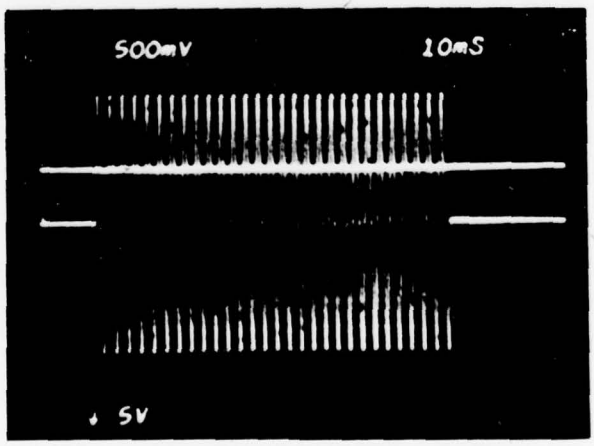
"0" VOLTAGE TURN ON
"0" CURRENT TURN OFF
INTO RATED LOAD CURRENT =
50 MA/CM

Figure 32.



TIME TRIP @ 200% RATED LOAD
SIGNAL = 2A/CM
CONTROL @ 5 V/CM

Figure 33.



TIME TRIP @ 500% RATED LOAD
SIGNAL = 5A/CM
CONTROL @ 5 V/CM

Figure 34.

SECTION IV

TEST PROGRAM

4.1.0 SUMMARY

The Appendix contains the detailed requirements of the job as listed in the Revised Statement of Work.

Failure Mode and Effects Analysis (FMEA), Transient Radiation Effects on Electronics (TREE), and Electromagnetic Pulse requirements. (EMP) testing have been performed on units in accordance with the requirements of the test plans which had previously been submitted to AFAPL.

The Qualification Test Program submitted to AFAPL was written in accordance with the General Design Specification of AC Solid State Power Controller, Appendix A, November 30, 1973 and carried out during the period of March 1977 to May 1977.

There were no deleterious effects due to EMP and the Power Controller proved to have sufficient hardness to operate properly during and after the exposure.

The Failure Mode and Effects Analysis plus the Transient Radiation Effects on Electronics analysis are summarized in Sections 2.2 and 2.3. The power controllers were exposed to gamma and neutron fluence radiation levels in accordance with the Rockwell Specification L409C2010.

Two units were exposed to delayed gamma tests at specified levels and proved to have sufficient hardness against the specified dosage. All three units exposed to the prompt gamma test also proved to have sufficient hardness to survive the specified dosage. Two of the three experienced a nuisance trip during exposure. Corrective action for this marginal operation is detailed later.

Component testing revealed some degradation in the opto isolators due to neutron fluence tests. Further testing led to the choice of a PIN diode opto isolator which was incorporated in units that successfully passed the neutron fluence tests performed at IRT Corporation, by a factor of 10.

4.2.0 QUALIFICATION TESTS

The Qual Test Program as outlined in table 1 provided adequate assurance that the Solid State Power Controller, (SSPC), would meet the electrical and environmental requirements of the B1 or any equivalent aircraft. Details of tests performed at out-of-house facilities are enclosed in a separate report.

TABLE 1

SCHEDULE OF TESTS

GROUP I	DESCRIPTION	SAMPLE NO.			
Test No.		1	2	3	4
1	Visual Inspection	X	X	X	X
2	Control/Reset Input Voltage	X	X	X	X
3	Control/Reset Input Current	X	X	X	X
4	Control Input Transients	X	X		
5	Control Input Noise Immunity	X	X		
6	Overload Trip Indication	X	X	X	X
7	Turn On and Turn Off Times			X	X
8	Isolation	X	X	X	X
9	Output Voltage Drop	X	X	X	X
10	Output Leakage Current	X	X	X	X
11	Waveform Distortion	X	X	X	X
12	Operating Voltage Transients	X	X		
13	Zero Voltage Turn On, Zero Current Turn Off			X	X
14	Trip Out Time	X			X
15	Power Dissipation	X	X	X	X
17	Radio Interference (Outside Testing)				
18	Removal Time to Reset	X			X
19	DC Offset Voltage	X	X	X	X

Table 1 (Cont)

GROUP I	DESCRIPTION	SAMPLE NO.			
Test No.		1	2	3	4
20	Trip Free Characteristics	X			X
21	Load Compatibility		X		
22	Rupture Current		X	X	
GROUP II	ENVIRONMENTAL TESTS	SAMPLE NO.			
Test No.		1	2	3	4
23	High Temperature	X			
24	Low Temperature	X			
25	Thermal Shock		X		
26	Moisture Resistance		X		
27	Insulation Resistance	X	X	X	X
28	Dielectric Withstanding Voltage	X	X	X	X
29	Salt Fog	X			
30	Shock (Outside Testing)	X			
31	Vibration (Outside Testing)		X		
32	Acceleration (Outside Testing)		X		
33	Attitude (Outside Testing)	X			
34	Explosive Decompression (Outside Testing)		X		
GROUP III					
35	Seal (Outside Testing)			X	X
36	Life			X	X

Two minor problems were encountered during Random Vibration and the Moisture resistance Test. Nine hours of sinusoidal vibration on 3 axis, 30 minutes of random vibration on the vertical axis plus 18 minutes on a horizontal axis had been run prior to a failure. When the unit was opened an open "J" pin connection as shown in figure 35 was found at a connection between the flexprint and the power supply circuit card assembly. A close look at the joint through a magnifying glass revealed that it had not been heated enough to allow the solder to properly flow. This particular connection is partially obscurred and the corrective action that has been taken is the use of better lighting and increased inspection at critical fabrication points.

During the last cycle of a Moisture Resistance test a dielectric withstanding voltage test was performed. A leakage current greater than the specified 1ma. maximum flowed. The unit was opened and the Hi Pot current flow was isolated to the connector assembly. The photographs in Figure 36 taken through a microscope, show conductive particles contaminating the area between the connector pins. These particles were probably aligned during the vibration portion of the Moisture Resistance test thereby providing the unwanted path for current. After a thorough investigation of assembly techniques, processes, and materials used in the power controller, it was concluded that the metal particles came from an external source. To preclude the possibility of future contamination due to handling, the connectors are being kept covered until installation. At that time another inspection is performed which insures contamination free fabrication.

During CS02 and RS03 EMI testing four descreet frequencies, two of which were at levels marginally close to specification, caused the unit to trip out. Additional susceptibility testing at the EMI test facility allowed further investigation into the cause of the problem. Convenience and readily available expertise then made it more desireable to continue the testing in house rather than at the test lab. It was found that by adding a break point at 100 KHZ on the I.P. and I.N. lines leading to the trip flip flop, the susceptibility problem was eliminated. No other electrical parameters were effected by this addition.

Several isolated points were beyond specification levels during conducted and radiated emissions. Additional circuitry is needed as in the previous case but the present configuration prohibits these additions from being made in an economic and timely manner.

A future iteration of the SSPC will accommodate circuitry which will eliminate these minor deviations.

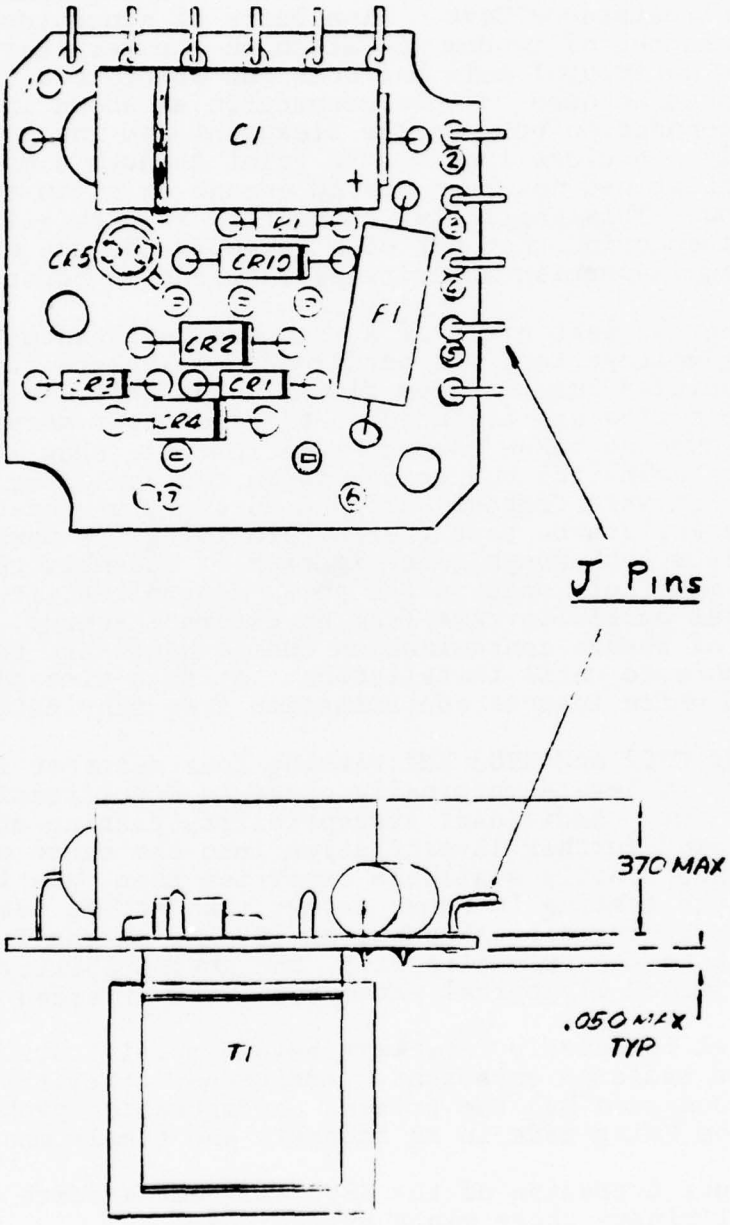
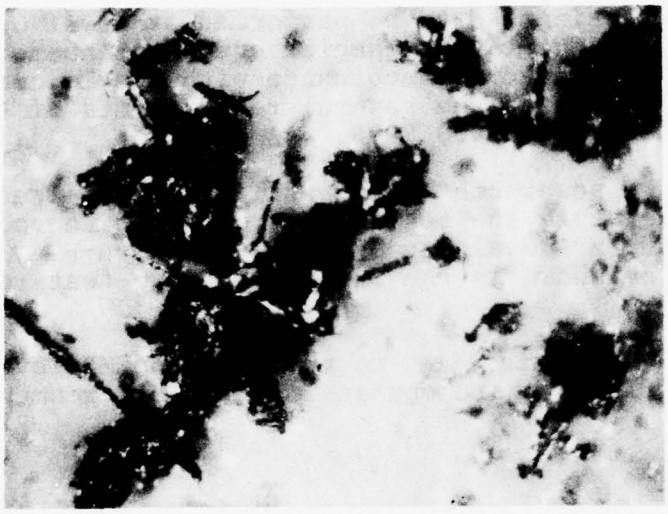


Figure 35. Power Supply Assembly Detail



APPROXIMATELY
25X
MAGNIFICATION

APPROXIMATELY
10X
MAGNIFICATION

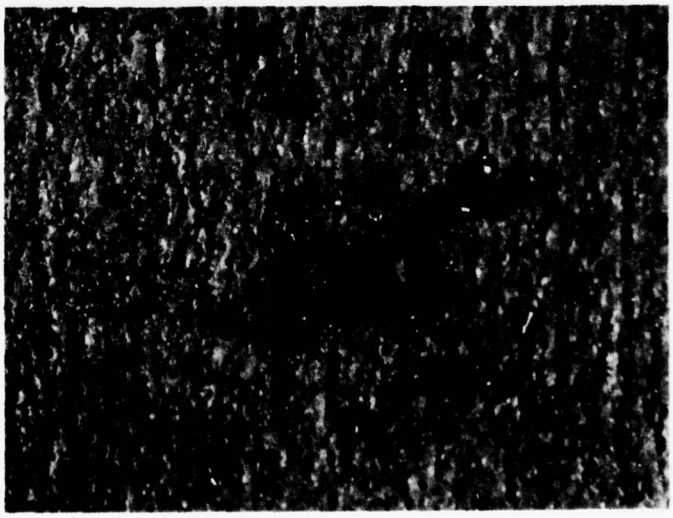


Figure 36. Shavings Found Inside Connector

4.2.1 EMP SUMMARY

This special type of testing had to be performed at Naval Ordinance Lab, White Oaks, Maryland due to the complex equipment needed to run the test. The test was performed in accordance with the Telephonics EMP Hardness Evaluation Test Plan and the general requirements of the Rockwell International specification L409C2005.

The construction of the power controller utilizes a shielded conductive enclosure, and therefore the testing was confined to cable Transient effects. Simulated EMP level signals shown in Figure 37 were coupled into the cable as shown in the Dayton T. Brown test report under separate cover.

The SSPC revealed no susceptibility to the induced EMP level pulses thereby providing sufficient hardness against EMP environmental conditions.

4.2.2 TREE TEST SUMMARY

A comprehensive program of analysis and subsequent testing was performed on the SSPC at both component and prototype levels. Detailed test results are classified and are contained in a separate report. The analysis was included in the Interim Technical Report.

The nuisance trip problem mentioned in section 4.1.0 has been investigated. A solution to this marginal problem is to add some additional capacitance to the FET outputs of the CMOS chip in the trip circuit. This makes the trip circuit insensitive to the effects of prompt gamma radiation tests, but in no way compromises any desireable circuit or unit parameters.

In this iteration of the SSPC it is not possible to make this modification since the outputs of the CMOS chip are buffered and are not brought out of the chip on pins.

Component testing led to the replacement of the Spectronics opto isolators with Hewlett Packard opto isolators since the Spectronics units degraded substantially during exposure to neutron fluence tests. With the new isolators installed, two units were subjected to the neutron fluence test and operated successfully at up to 10 times specification level.

In all the SSPC has displayed sufficient hardness to survive neutron fluence, delayed gamma, prompt gamma exposure, with no degradation of their operational parameters.

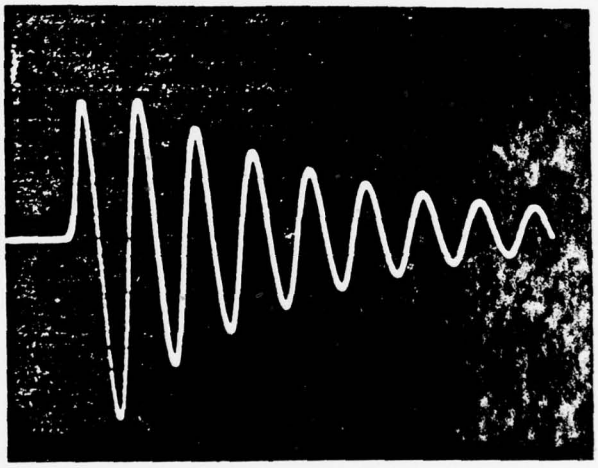


Figure 37. Typical EMP Induced Waveshape

4.3.0 FAIL SAFE

A special test fixture as shown in figures 38 and 39 was developed in order to be able to apply the specified Fail Safe current of 1200 Amps peak, along with a surge current also with a 1200 Amps peak. The links were tested in accordance with the General Design Specification requirements and the waveforms in figure 40 reveal typical results of these tests. All four waveforms have a time base of 1 millisecond per centimeter and an amplitude of 200 amps per centimeter. Figures 40A and 40C show the test fixture capability with the test fuse short circuited. Figures 40C and 40D reveal the results of allowing the high currents to flow through the fuses. In 40B we see that the full peak current never flows, but that an apparent arc is sustained for several milliseconds before extinguishing. In Figure 40D again the peak current is not attained, but an arc is sustained, proportional to the voltage applied, for approximately 7 milliseconds. In each case the arc extinguishes prior to the voltage reaching zero. Immediate retest revealed the fuses to be open.

The fuses perform the job of being able to interrupt very high currents, but because of their miniature size there is the possibility that adjacent circuitry can be destroyed. This can occur during the blow time since the arc may not be contained in either of the ceramic or metal can type miniature fuses. Tests on larger 8AG type instrument fuses revealed superior characteristics such as shorter arc times and completely contained arcing. Figure 41 shows the typically shorter arc times, (approximately 1.4 MS), associated with physically larger fuses.

4.4.0 CONCLUSIONS

4.4.1 ELECTRICAL -

The extensive electrical test program proved fruitful in that the SSPC meets or exceeds all the electrical parameters required by the General Design Specification.

4.4.2 ENVIRONMENTAL

The mechanical configuration and assembly techniques used in the unit proved sufficiently rugged to withstand the full spectrum of required environmental testing.

4.4.3 EMI

EMI testing revealed certain problems within the present configuration. A series of tests conducted outside and in house led to available solutions in the most critical areas.

4.4.4 EMP & NUCLEAR RADIATION

The SSPC displayed sufficient hardness to survive simulated nuclear weapon induced EMP levels, gamma radiation, and neutron fluence tests at specified or greater than specified levels.

4.4.5 FAIL SAFE

Evaluation of the fuses selected for use in the SSPC determined that they had the capability of breaking extremely high currents, but also revealed the undersireable characteristic of the possibility of an uncontained arc. In the present hermetically sealed configuration this is not a problem since there is a negligible possibility of fire.

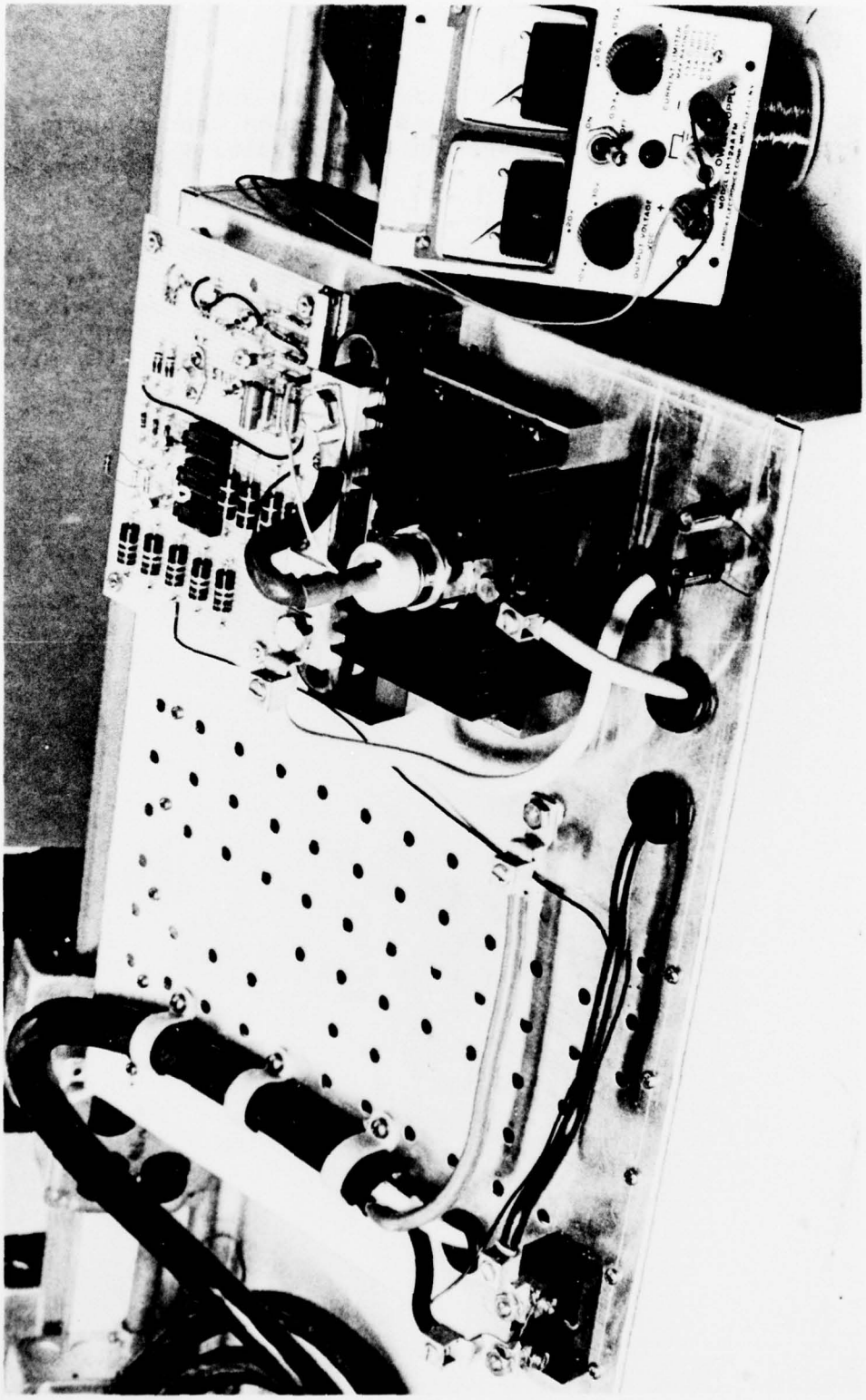


Figure 38. Fuse Test Fixture

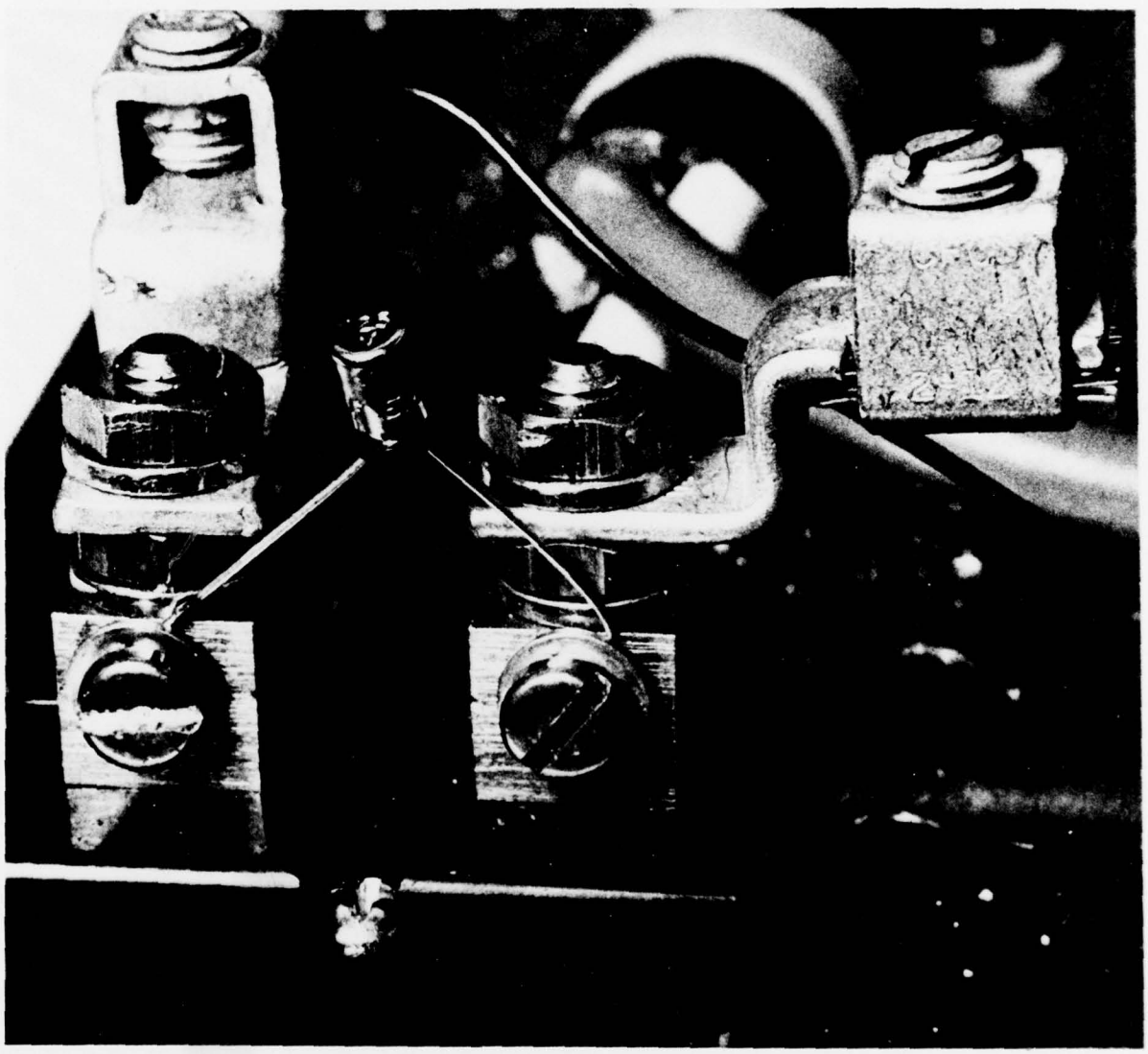
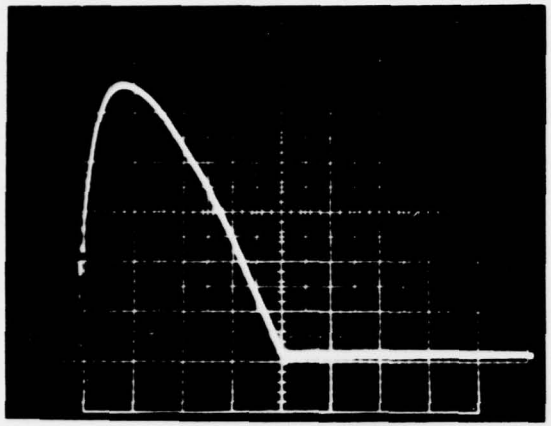
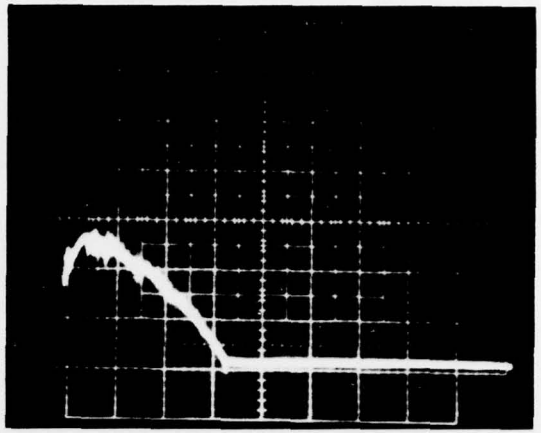


Figure 39. Fuse Test Fixture Detail

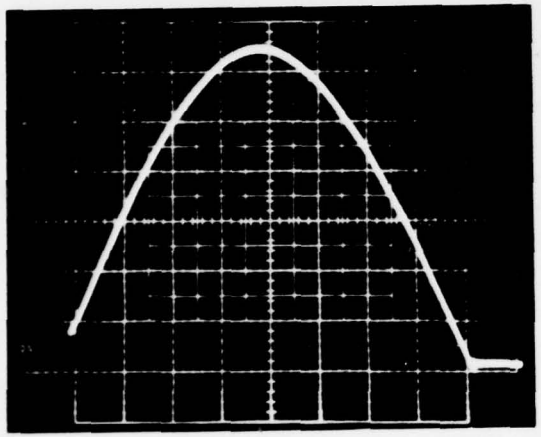
A



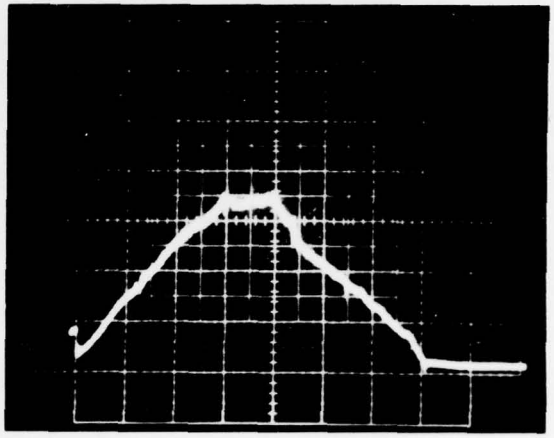
B



C

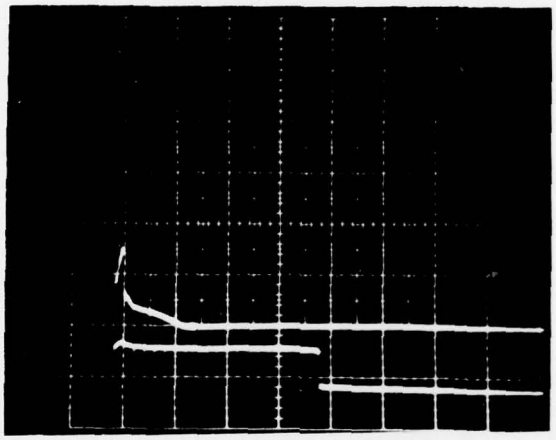


D



200 AMPS/CM - 1MS/CM

Figure 40. Fail Safe Fuse Currents



200 AMPS/CM - 1 MS/CM

Figure 41. Fail Safe Fuse Currents

SECTION V

RECOMMENDATIONS

a. A general study should be performed on the suitability of cans or printed circuits, for aircraft of various sizes and complexities. In many cases, a printed circuit card configuration should be considered instead of the hermetically sealed can, for the following reasons:

1. The hermetically sealed modified IWTS connector used in the can is expensive, has a very limited number of allowed insertions and withdrawals, is a potential source of hipot failures, numerous other problems.

2. a printed circuit card is repairable, whereas a sealed can must be discarded if it fails.

3. The quad pc card weighs significantly less than four sealed cans (11 ounces vs 16 ounces).

b. Common returns could be used for the input control signals and the output trip signal (and status signal, if used). This would reduce internal complexity in the power controller, as well as the number of wires between the power controller and the EMUX.

c. The source impedance of the 400 HZ generator, including the line, current transformer, feedthrough or other filter capacitors, etc., should be completely specified. It should be noted that a minimum as well as maximum inductance is very significant, as well as the maximum capacitive component of the source.

d. Do not commit the design to use special connectors that are volume restrictive and costly.

e. With the prospect of continued advancement of transistorized power controllers, all possible encouragements should be made to manufacturers for development or transistor devices with higher current and voltage ratings.

APPENDIX

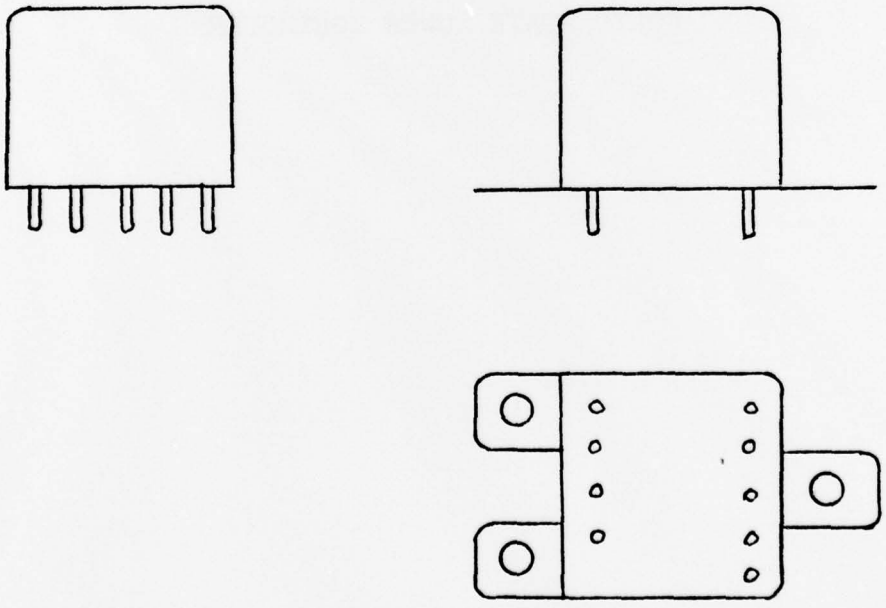
GENERAL DESIGN SPECIFICATION FOR AC SOLID STATE POWER CONTROLLERS

SPECIFICATION SHEET

Power Controllers designed to this spectification are double voltage devices. The power source quality shall be per MIL-STD-704 and Curve 1 herein.

TERMINAL IDENTIFICATION

TERMINAL	FUNCTION
Power Controller, AC Load Switching SPST, Normal Open, 1.5 Ampere, 230 Volt	Power In
	Power Out
	Power Ground
	Control
	Control Ground
	Trip Indication
	Trip Ind. Return
	Status Indication
	Status Ind. Return



PROPOSED PACKAGE CONFIGURATION
FIGURE 5

REQUIREMENTS:

MECHANICAL AND DIMENTSIONAL CHARACTERISTICS

Configuration	See Figure 5
Dimensions	Inches
Tolerances	± 0.02 for two place decimals ± 0.005 for three place decimals
Enclosure	Hermetic Seal
Weight	3.0 Ounces Maximum
Mounting Torque	15 in. lb.

THERMAL CHARACTERISTICS

Thermal Resistance Case-to-Sink	0.5°C/watt with specified mounting torque
Heat Sink Temperature (Design Consideration)	77°C maximum

ELECTRICAL CHARACTERISTICS (-54 to 75°C case temperature unless otherwise specified)

GENERAL

Terminal Arrangement	SPST (normally open)
Insulation Resistance	100 megohm minimum
Dielectric Withstanding Voltage	Applicable (1500V rms, 60 Hz, 5 sec.)
Isolation	Applicable Between control, status, trip shorted and output terminals shorted, (1500 Vrms, 60 Hz, 5 sec.) Between control, status and trip circuits - (300Vrms, 60 Hz, 5 sec.)
Life (operating cycles)	10^5 minimum
Radio Interference	Applicable
Leakage Current	1.0 milliampere maximum at rated voltage
Power Dissipation (max @25°C ambient)	
'ON' - rated load	4.0 watts (see Figure 3)
'OFF'	0.50 watts

POWER CIRCUIT

Supply Voltage	244 volts rms maximum
Limits 1 and 6 of Curve 1	208 volts rms minimum
Current	
Rated	1.5 Ampere
Frequency (rated)	400 Hz ± 5%
Voltage Drop (see Figure 1)	2.2 volts rms maximum (room ambient and above)
Rupture Capacity	320 Amperes Peak

Waveform Distortion	2.2 volts rms and 6.0 volts peak max.
DC Offset Volts Maximum	No Load - 1.0 volts 10% to Rated Load - 0.1 volts
Fail-Safe	640 Amperes Peak
Transients	
Operating Voltage	Applicable
Response	
Turn-On Time (from application of control)	5-15 MS
Turn-Off Time (from removal of control)	5-15 MS
Trip-Free	Applicable
Trip-Out Time	Applicable
Nonrepetitive Reset	Applicable
Repetitive Reset	Applicable
Trip Indication (Table 1.0)	
Signal Sw. open (not tripped)	0.025 ma, max. leakage
Signal Sw. closed (tripped)	1.0V dc, max. drop at 2.0 ma or 1.5V max drop at 10 ma
Status Indication (Table 1.0)	
Signal Sw. open (main sw. open)	30Vac max. 0.025 ma max. leakage
Signal sw. closed (main sw. closed)	1.0Vdc max. drop at 2.0 ma 1.5V max drop at 10 ma
Zero Voltage Turn-On	Applicable
Zero Current Turn-Off	Applicable Full Cycle Control

CONTROL CIRCUIT

Supply Voltage	+6.0 volts dc maximum +5.0 volts dc rated
Turn-On Voltage	+4.0 volts dc minimum
Rise Time	1.0 microseconds minimum
Turn-Off Voltage	+2.0 volts dc maximum
Rise Time	1.0 microseconds minimum
Input Control Current	10.0 ma max @ 6.0 volts
Input Resistance	1000 Ohms maximum
Input Transients	Applicable
Noise Immunity	Applicable
Reset	By removing & reapplying the dc control voltage
Time to Reset (removal)	5.0 milliseconds minimum 20.0 milliseconds maximum

ENVIRONMENTAL CHARACTERISTICS

Case Temperature	
Operating	-54°C to +75°C
Storage	-65°C to 95°C
Shock	
Mechanical	40G for 11 ± 1.0 milliseconds
Temperature	-54°C and +71°C ambient

Vibration	Applicable
Sinusoidal (operating)	
G Level	15G maximum
Frequency Range	5-2000 Hz
Random: (operating)	
Power Spectral Density	$0.2G^2$/Hz maximum
Frequency Range	20-2000 Hz
Acceleration	100G
Salt Fog	Applicable
Humidity	Applicable
Temperature-altitude	Applicable
Operating ambient	
Temperature	-54°C to +71°C
Altitude	Sea level to 100,000 feet
Non-operating ambient	-65°C to +95°C
*Operating ambient	
Normal & extended emergency conditions	-54°C to +71°C
Emergency - 10 minute duration	-54°C to +95°C
Altitude	0.65 to 15.4 PSIA
Explosive decompression	11.1 to 0.65 PSIA in .01 sec. at 1,045 PSI/sec minimum

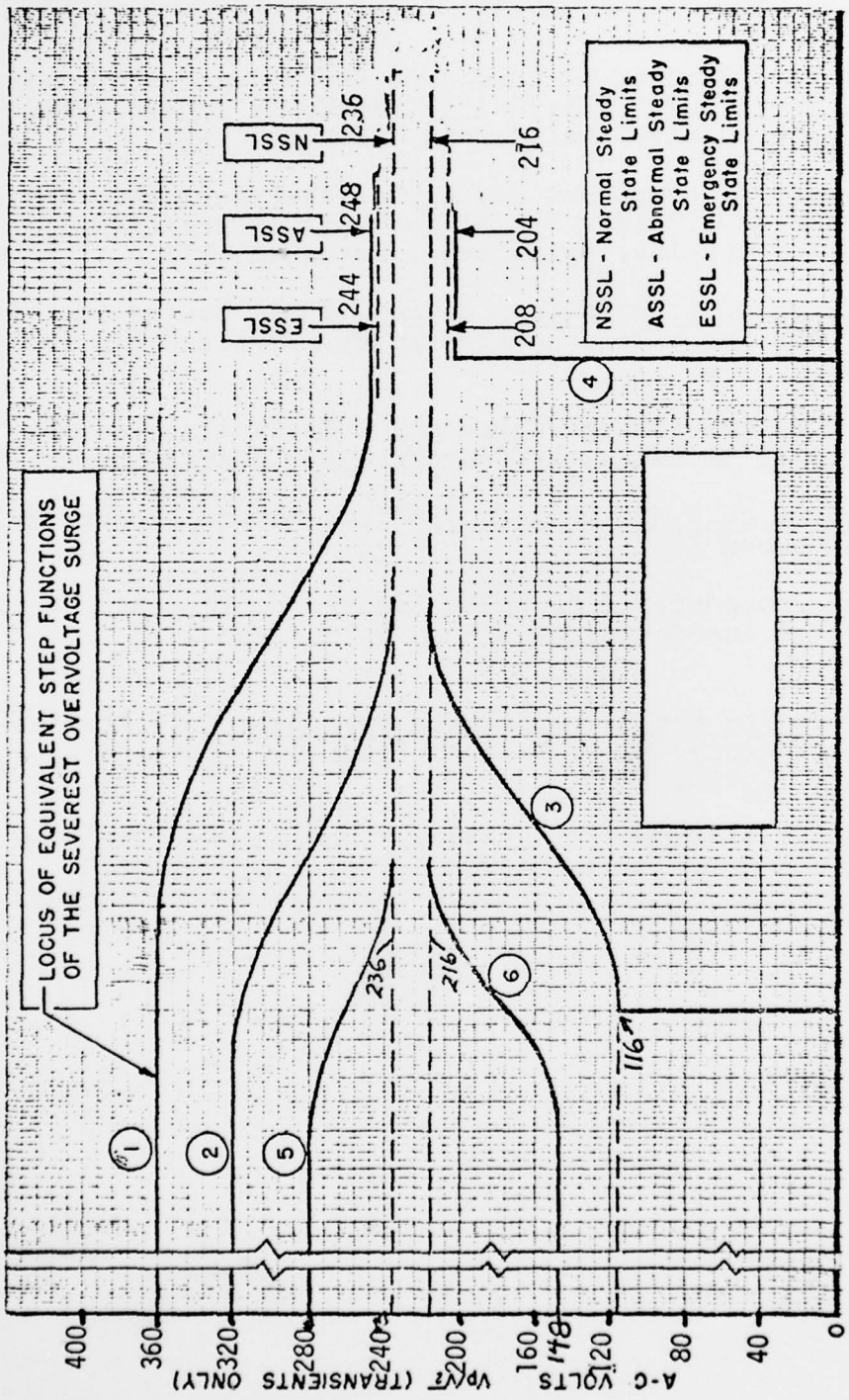
*6.0°F/sec. maximum rate of temperature change

SIGNAL INDICATION PERFORMANCE

ITEM	"PC" CONDITION	LINE VOLTAGE	CONTROL VOLTAGE	TRIP INDICATION	LOAD VOLTAGE	STATUS INDICATION
1	"On State" Normal	Present	Present	Signal Switch Open	Present	Signal Switch Closed
2	Overload in Non-Trip Region	Present	Present	Signal Switch Open	Present	Signal Switch Closed
3	Load Voltage is Removed Due to Tripping	Present	Present	*Signal Switch Closed	Absent	Signal Switch Open
4	Step 1 of Reset: Control Voltage Removed	Present	Absent	Signal Switch Open	Absent	Signal Switch Open
5	Step 2 of Reset: Control Voltage Re-applied (See Item 1)	Present	Present	Signal Switch Open	Present	Signal Switch Closed

*"Trip Indication Switch" remains "ON" until "control voltage" is removed as step 1 of reset operation.

TABLE 1.0



Double Voltage AC Power, Transient Surge AC Voltage Step
Function Loci Limits for Category B Equipment
CURVE 1

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